CONTROL OF THE LOW LEVEL RF SYSTEM FOR THE J-PARC LINAC

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Abstract

The J-PARC 181-Mev proton linac requires twenty-four RF systems, which operate at a 620-μs pulse width, 50-Hz repetition rate, and 324-MHz frequency. The required basic functions of the low level RF (LLRF) control system for the klystron RF source are: field control, high-power protection, analog and status monitor and klystron drive. To perform these functions a programmable logic controller (PLC) is used as the main system controller. The PLC will be locally operated by a touch panel on PLC LAN and remotely by an EPICS Operator Interface (OPI) on EPICS LAN. This paper describes the LLRF hardware configurations and the system control using the PLC.

INTRODUCTION

The RF source of the J-PARC 181-MeV proton Linac is composed of four solid-state amplifiers and twenty klystron amplifiers. In each RF source, the cavity field will be stabilized within an accuracy of ± 1% in amplitude and ± 1° in phase. This field control, which is implemented by a combination of feedback (FB) and feed-forward (FF) algorithms, is the most important key function in the low level RF (LLRF) system, and requires much of our efforts [1][2]. However, seeing from the viewpoint to control the whole LLRF system, the field control is one embedded system, all of the LLRF components, such as a high power protection unit, status and analog monitors and a klystron driver, are controlled by a system controller with interfaces for local and remote operation. We adopt a programmable logic controller (PLC) as the main system controller.

OVERVIEW OF THE LLRF SYSTEM

There are twenty-four LLRF systems corresponding to each of the solid-state and klystron amplifier stations. A block diagram of the LLRF system for the klystron station, including an interface with the EPICS control system (VME/IOC and NIM/Timing), is shown in Figure 1. The required fundamental functions for the LLRF system are: 1) generation of the accelerating RF (324 MHz) and clock (12 MHz, 48 MHz and 312 MHz) signals phase-locked with a 12-MHz optical signal provided with the rf reference distribution system [3], 2) cavity field and tuning control (cPCI/Digital FB), 3) high-power protection and RF monitor (Fast Interlock, Arc Detector and VSWR Meter), and 4) klystron drive (Analog FB, 20-dB and 40-W amplifiers).

The signal generation and the cavity field and tuning control are performed by a cPCI crate system, which is composed of a host CPU module, a control input/output module (CTRL I/O), a mixer and I/Q modulator module (MIX&I/Q-M), a DSP module attached with a FPGA mezzanine card, and an RF and clock generator module (RF&CLK). All of the LLRF hardware components which are listed in Table 1 are installed in two 19”

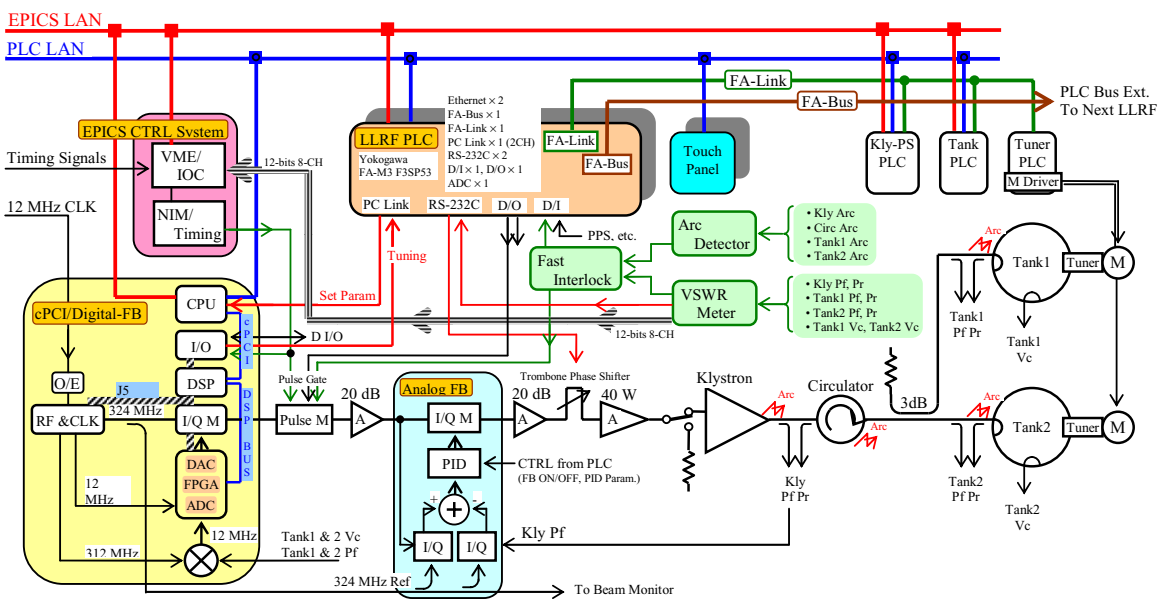

Figure 1: Block diagram of LLRF System.

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standard racks (1400W × 800D × 2000H).

Table 1: LLRF hardware components and their unit size

Chassis Unit	Height (unit)	
PLC and Touch Panel	7	Touch Panel mounted on PLC chassis front panel
cPCI Crate	8	covered with noise-shield case with fans
NIM Bins	5 × 2	Pulse Mod, 3-CH 20-dB Amp, Fast INT, Arc Detect., Analog FB CTRL, Osc. Trig Delay
VSWR Meter	3	with peak power meter function
40-W Amp.	4	include dc power supply
40-W Output Unit	2	monitor couplers, circulator, coaxial SW
Tromb. Phase Shifter	side panel	motor driven (20 cm × 80 cm)
Temp. Module Panel	rear panel	4 thermocouple modules
I/O Connector Panels	3 × 2	main purpose for ground sink
1-GHz Oscilloscope	7	waveform and phase read-out
Others	10	2 fan units, MCCB

CONTROL COMPONETS OF THE LLRF SYSTEM

The components for controlling the LLRF system, as shown in Figure 1, are the PLC, Touch Panel, EPICS Control System, cPCI System, and Fast Interlock. The hardware configuration and control function for each of these components are described as follows:

PLC

Though it isn't shown in Figure 1, there are two types of PLCs: a main unit which has a CPU module in its back plane bus, and a subunit which doesn't have a CPU and is connected on the expansion bus of the main unit by an FA-Link module. The main unit is one rate in four systems, thus, one CPU works four system tasks. Figure 1 shows the case that PLC is a main unit. Differences between the subunit and the main unit are two points: the subunit has no connection to LANs and no link with other PLCs. All others are similar system configurations. The followings are explained about the system whose PLC is a main unit, as well as the paragraph mentioned above.

The modules used in the PLC are shown in Figure 1. Control functions of the PLC can be depicted in Figure 2. In order to operate the system and provide remote and local access to the PLC, there are the EPICS VME/IOC and the Touch Panel (TP). Two types of modules for serial (RS-232C) communication are used: one is a 2-channel PC-Link module which is implemented by a client program for communication with the cPCI/CPU module and the cPCI/DSP module routed through the cPCI/CTRL I/O module, and the other is Ladder Program Communication modules which are implemented by PLC ladder programs for communication with the VSWR Meter and the Trombone Phase Shifter. As a control output from the PLC, ON/OFF commands are transmitted to the cPCI/FPGA through the cPCI/CTRL I/O, Pulse Modulator, Klystron Input SW, and Analog PID. In addition parameter settings are transmitted to the Tuner PLC, cPCI/CPU, Analog PID, and Trombone Phase Sifter.

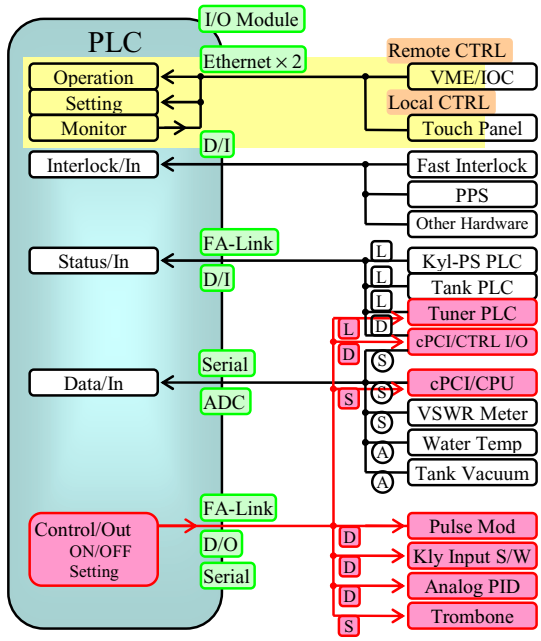

Figure 2: Control flow from/to the PLC.

Touch Panel

The Touch Panel (TP) provides a GUI for local operation and all the functions necessary to control the entire LLRF system. In addition important data such as the field amplitude and phase, the cavity tuning angle and vacuum, and the klystron output power are displayed in the trend graph.

EPICS VME/IOC

The EPICS VME/IOC is an I/O interface with EPICS which is supported by the linac control group. The PLC is remotely controlled by reading and writing from EPICS to the PLC register. The required timing signals for the LLRF system are provided by the EPICS NIM Timing system. In addition the high-refresh-rate dada from the VSWR Meter (8-CH 12-bit, 50 Hz) are saved in to the EPICS database.

cPCI System

The cPCI system composed of five modules and one mezzanine board (FPGA) is shown in Figure 3. In these modules only the CPU and DSP modules utilize the PCI system bus (J1 and J2), while the other modules utilize only the user bus (F3 and J5) and, thus, merely make use of its standard module case. The boards (CPU, DSP, FPGA and CTL I/O) relevant to control are explained as follows:

A *CPU* module used as a cPCI system host is a general purpose Pentium CPU board (ACP-128-1, AVALDATA Co., PentiumM/1.6GHz). On the front panel the PC standard communication and device I/O ports, such as Ethernet (×2), COM, keyboard, display and etc., are provided, which make it easy to locally debug and diagnose the software and system. The COM port is used for the communication of all the control data required for

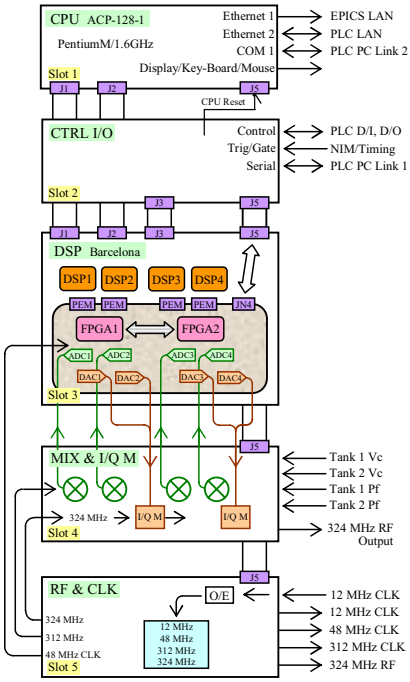

Figure 3: Block diagram of the cPCI modules.

the field control from/to the PLC. One Ethernet port is for the transmission of waveform data to the EPICS OPI as a FTP server. Another Ethernet port is connected to PLC LAN and served the network boot and the download of DSP execute and FPGA configuration files.

We adopt a Barcelona *DSP* board (Spectrum Signal Processing Inc., TMS320C6701 × 4). Each of the DSPs has an I/O port called "PEM" on the board which provides a high-speed dataflow (400 MB/s) from/to a mezzanine board inserted into the PEM connectors. The waveform data from the mezzanine (FPGA) board can be stored directly in lots of memories (512-kB SSRAM, 16-MB SDRAM) on each DSP local bus by a DMA engine, and, after processed by DPSs, transferred to the host memory on the PCI memory address space.

Besides J1 and J2 this DSP board has the J3 and J5 user bus connectors: J3 is for DSP global interrupts and serial communication, and J5 for user free I/O lines, which route a path to a 64-pin connector (JN4) on the board. We use JN4 as a signal path from the CTRL I/O to FPGA boards.

The *FPGA* board installed on the DSP board as its mezzanine board consists of two FPGAs (Xilinx Virtex-E XCV600E (FG676)), four ADCs (AD6644) and four DACs (AD9764). By equipping the FPGA board with all the PEM and JN4 ports, we obtain the expansible usability. The configuration PROMs on the board can be rewritten through the DSP serial port in the PEM ports, as well as the JTAG port, therefore we can download FPGA configuration files sent from the PC server on PLC LAN.

The Control I/O *(CTRL I/O*) board provides the signal paths from the PLC and NIM/Timing to the J3 and J5 cPCI user bus connectors. The digital I/O signals between the PLC and J5 bus are RF ON/OFF, FB ON/OFF, fault latch Reset, host CPU Reset, FPGA OK, DSP OK, etc. The timing signals are FPGA pulse control Start/Stop, RF ON Gate, Beam ON Gate, Beam Chopper Clock (~1 MHz), etc.

Fast Interlock

In order to protect the high-power components such as RF windows in case of RF discharge and over RF reflection, we must shut off the RF drive to the klystron as soon as possible. The Fast Interlock (Fast INT) module provides the high-power protection function by controlling a gate signal to the RF switch of the Pulse Mod module. The Fast INT module has many input signals, as shown in Figure 4: four arc detection signals from the Arc Detector (klystron, circulator, tank-1 input port and tank-2 input port), three set signals of an over forward power (Pf), over reflection power (Pr) and VSWR (5-μs delay for processing) from the VSWR Meter, and the RF Out Enable signal from the machine protection system (MPS).

The Fast INT module also has an output function of the "RF Acc OK" signal which informs the RF source ready for beam acceleration to the MPS.

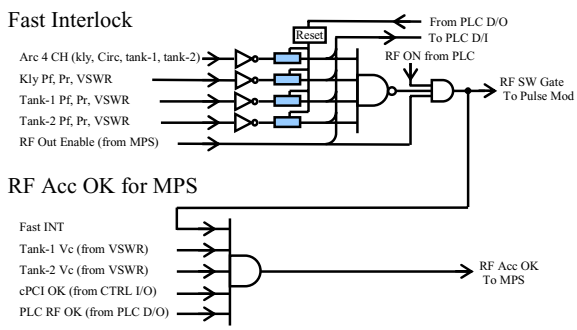

Figure 4: Block diagram of the Fast Interlock module.

CURRENT STATUS

Two prototypes of the LLRF system based on analog feedback have been operated at the DTL-1 RF station and the SDTL high-power test station in the 60-MeV test linac. All twenty-four LLRF systems will be delivered at the end of March 2005. We are developing the PLC program which includes the auto-recover process from fault down and the auto-conditioning process for cavities.

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