LLRF CONTROL UNIT FOR SuperKEKB INJECTOR LINAC

Takako Miura†1, Mitsuo Akemoto[1], Dai Arakawa, Hiroaki Katagiri, Toshihiro Matsumoto[1],
Feng Qiu[1], Yoshiharu Yano, KEK, Tsukuba, Japan
Na Liu, [1]Sokendai, Hayama, Japan

Abstract

The low-level RF (LLRF) control unit based on the digital system has been developed for a stable and high precision pulse modulation for the SuperKEKB. The RF pulse is changed at a 50-Hz repetition rate for the top-up injection to four different rings by the event system. The LLRF control unit has not only the pulse modulator, but also other functions: VSWR meter, RF monitor, event receiver (EVR), and pulse-shortening detection.

INTRODUCTION

SuperKEKB is an upgraded machine of the KEKB e-/e+ collider and aims at a 40-times higher luminosity than the KEKB by the nano-beam scheme [1]. The injector linac has also been upgraded to provide higher bunch charge and higher quality beam [2] for SuperKEKB.

Furthermore, the linac needs to provide the beams with top-up injection to four storage rings, not only the SuperKEKB HER/LER, but also the photon factory PF/PF-AR. Figure 1 shows the layout and beam energy patterns of the injector linac. The beam mode is switched pulse by pulse at a 50-Hz repetition rate of the linac, according that, the RF phase is switched for the each pulse by the event system [3]. The RF phase-inversion timing for the pulse compression is important to reduce the beam acceleration energy jitter, and it should be synchronized with the beam timing generated by the event-timing system.

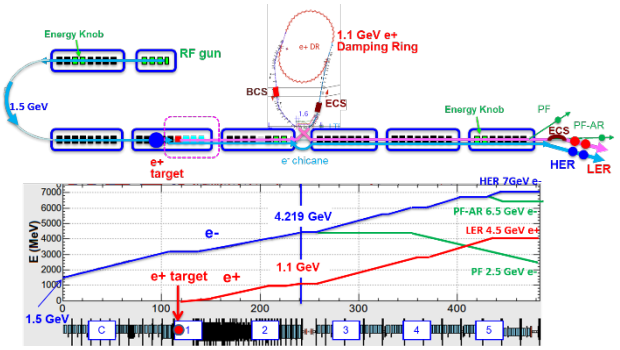

Figure 1: Layout and beam energy patterns of KEK injector linac.

For these purposes, various low-level RF (LLRF) components have been also upgraded [4, 5]. The new LLRF control unit based on the digital system has been developed for a stable and high precision pulse modulation for the SuperKEKB, and synchronization with the event system. During the upgrade construction, the linac had to continue providing the beam to the photon factories. Therefore, the new system was designed to be compatible with the previous system [6] for an easy replacement. This paper describes the LLRF control unit and its performance.

† Takako.miura@kek.jp

RF SYSTEM

As shown in Fig. 1, the linac is divided into eight sectors (A–C and 1–5). Figure 2 shows the RF drive-line. Each klystron unit consists of an S-band 50-MW klystron, which is operated at 40 MW, and a SLED [7], which is a pulse compressor. The RF frequency is 2856 MHz, and the RF pulse width is 4 μs. The RF phase is 180° inverted at the last 1 μs for pulse compression by the SLED. Each klystron unit feeds the RF power into four 2-m accelerating structures, and the field is 21 MV/m. Typically, each sector has eight klystron units. The RF pulse with amplitude and phase modulation is amplified by 60-kW sub-booster klystron, and the amplified RF pulse is distributed to eight klystrons in each sector. The input RF phase and amplitude for each klystron unit downstream of the sub-booster is adjusted by a mechanical-type high power IΦA (isolator / phase-shifter / attenuator). At the special units used for the electron-gun, bunching, and energy adjustment, the RF is controlled independently at each klystron unit using an LLRF control unit and a 600-W solid state amplifier.

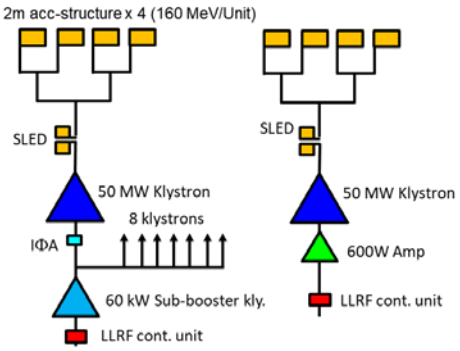

Figure 2: Klystron drive-line from a sub-booster klystron (left), and independent drive-line (right).

LLRF CONTROL UNIT

The new LLRF control unit has been developed since 2011[8] as a pulse modulator with a higher precision and stability than the previous one: further, it has additional functions such as a VSWR meter, RF monitor, event-receiver (EVR), and pulse-shortening detection.

Figure 3 shows a block diagram of the LLRF control unit. The control unit consists of a Xilinx Virtex-6 FPGA board, an analog-to-digital (AD) / digital-to-analog (DA) board (six 14-bit ADC: AD9254, six 14-bit DAC: AD9744) that is connected to the FPGA by an FMC connector, I/Q modulator/demodulator, and Armadillo CPU board with an

LCD touch panel. The sampling clock of the ADC/DAC is 114.24 MHz, which is the same frequency as the event-trigger system, to reduce the phase inversion timing jitter for the beam.

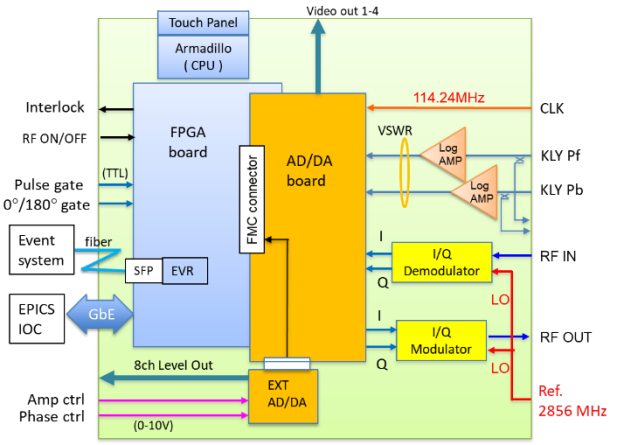

Figure 3: Block diagram of the LLRF control unit

The waveform data and some information are sent through a Gb Ethernet to the EPICS-IOC server at the 50-Hz repetition rate of the injector linac.

For the LLRF system upgrade, RF monitor units [5] have been developed, and a similar design with the control unit was adopted.

Figure 4: Front/rear panel of LLRF control unit

Figure 4 shows the picture of LLRF unit. The pulse trigger and four-channel "video signals" used for the oscilloscope inputs in the front panel are output by DACs. We can set the parameters not only by the front touch panel but also by the VNC remotely. The parameter settings are saved in the SD card on the CPU board, or the USB memory.

RF Pulse Modulator

The RF pulse timing and width, 0°/180° inversion timing, amplitude, and phase are controlled by external inputs. The external control inputs are generated by event system depending on the pulse mode changed at 50 Hz. In phase control, it has an "analog mode" and "digital mode". In the analog mode, which is the same as the old version, the phase is controlled by an external 0–10 V level input corresponding 0–400°. Meanwhile, in the digital mode, the phase information, which is distributed on an optical fiber from the event system, is received directly by the EVR implemented in the FPGA board. The digital mode is under testing. The RF pulse is generated by the I/Q modulator using I/Q baseband outputs from the DACs and a 2856-MHz LO signal.

The correction for the nonlinearity of the I/Q modulator is performed by calculations in the FPGA using the I/Q calibration table, which is stored in the compact flash memory on the FPGA board. The specifications of the RF pulse modulator are shown in Table 1

Table 1: Specifications of RF pulse modulator

Frequency	2856 MHz
RF output level	+10 dBm (100%)
Linearity of amp.	0.3% rms and max < ±0.5%
RF pulse rise time	< 35 ns (0 - 90%)
Phase setting-range	0 – 400°
Linearity of phase	0.3° rms and max < ±0.5°

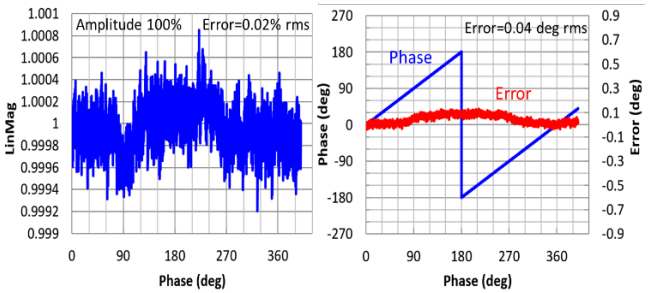

Figure 5: Amplitude and phase error of RF output

The typical result of the amplitude and phase accuracy of the RF output is shown in Fig. 5. The amplitude error is 0.02% rms and the phase error is 0.04° rms in an amplitude setting of 100%.

Figure 6 shows the measurement result of the temperature dependency of the RF output phase. The temperature was changed at 1 °C intervals, and the humidity was maintained at approximately 40% rh.

The output phase changed by approximately 4° between 22 °C and 28 °C. The temperature dependence of the phase is severely large, and the thermal coefficient is 0.62 °/°C. Thus, the LLRF control unit for each sub-booster has been installed in a thermostatic chamber. However, in the case of an independent drive unit, the temperature is not stabilized. This should be improved in the future.

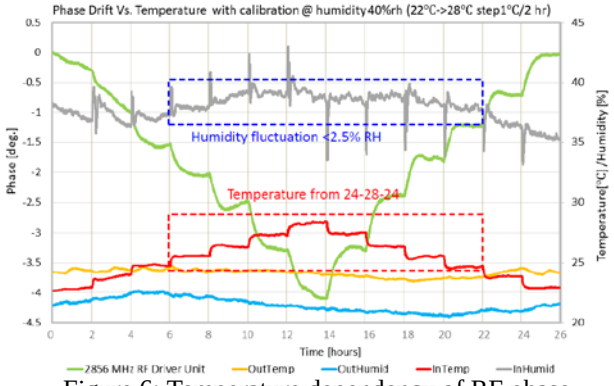

Figure 6: Temperature dependency of RF phase.

VSWR Meter

The LLRF control unit has the function of a VSWR meter for protection of the klystron RF window. Three gate ranges are prepared. The first two are to exclude the phase-inversion timing, and third is a special one to detect the delayed reflection due to the discharge of the far accelerating structure. In each gate, we can set each Pf, Pb, and VSWR level, and select the type of the interlock. Furthermore, the interlock level is switched in the high- or low-level mode for the threshold level, as shown in Fig. 7.

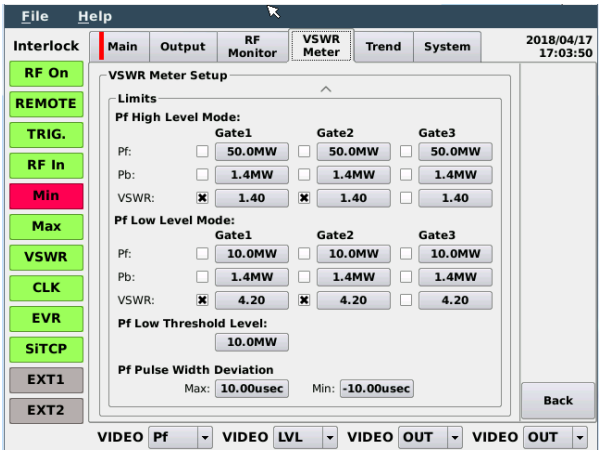

Figure 7: Settings panel of VSWR meter.

Pulse-Shortening Detector

Klystron pulse-shortening means that the width of the pulse becomes short, as shown in Fig. 8. It is caused by the inside of the klystron. In the LLRF controller, the pulse-shortening is detected by comparing the pulse gate width and the measured pulse width. When the pulse-shortening occurs, the VSWR interlock may occurs because of the low or zero forward power. In the case of the pulse-shortening, therefore, we can choose whether to disable the VSWR interlock. The information on the occurrence frequency is useful for evaluating the klystron performance.

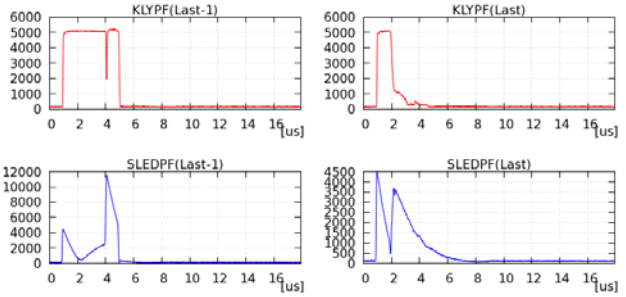

Figure 8: Klystron output (top) and SLED output (bottom). Left: Normal case, right: Pulse-shortening case.

SUMMARY

The LLRF control unit in the SuperKEKB injector linac has been upgraded for a stable and high precision pulse modulation. The RF pulse timing and phase are switched at 50-Hz depending on the beam mode for the top-up injection to four rings. The pulse modulation is controlled by the event system, and synchronizes with the event system clock to reduce the phase-inversion timing jitter against the beam.

The nonlinearity of the I/Q modulator was well corrected by the I/Q calibration. The phase drift depending on the temperature is severely large, i.e., 0.62 °/°C. Thus, the LLRF control unit for the sub-booster has been installed in a thermostatic chamber.

Furthermore, the LLRF control unit has other functions: VSWR meter, RF monitor, event receiver (EVR), and pulse-shortening detection, etc. All these functions are working well.

REFERENCES

[1] Y. Ohnishi *et al.*, "Accelerator design at SuperKEKB", *Prog. Theor. Exp. Phyes.* 2013, 03A011.

[2] T. Kamitani *et al.*, "Injector LINAC upgrade for SuperKEKB", in *Proc.* LINAC'10, Tsukuba, Japan, Sep. 12-17, 2010, MOP011, pp. 70-72.

[3] K. Furukawa *et al.*, "Pulse-to-pulse Beam Modulation and Event-based Beam Feedback Systems at KEKB Linac", in *Proc.* IPAC'10, Kyoto, Japan, May 23-28, 2010, TUOCMH01, pp. 1271-1273.

[4] T. Matsumoto *et al.*, "Low-level RF system for the SuperKEKB Injector LINAC", presented at IPAC'18, Vancouver, Canada, Apr.-May 2018, paper WEPAK017, this conference.

[5] H. Katagiri *et al.*, "RF Monitor System for SuperKEKB Injector Linac", presented at IPAC'18, Vancouver, Canada, Apr.-May 2018, paper WEPAK016, this conference.

[6] H. Hanaki *et al.*, "Low-power RF systems for the KEKB injector LINAC", in *Proc.* APAC'98, Tsukuba, Japan, Mar. 23-27, 1998, pp. 139-141.

[7] H. Matsumoto *et al.*," High power test of a SLED system with dual side-wall coupling irises for linear colliders", in *Proc.* PAC'93, Washington, USA, May 17-20, 1993, pp. 959-961.

[8] Y. Yano *et al.*, "Development of compact klystron drive system and RF monitor", in *Proc. 8th Annual Meeting of Particle Accelerator Society of Japan*, Tsukuba, Japan, Aug. 2011, pp. 620-623.