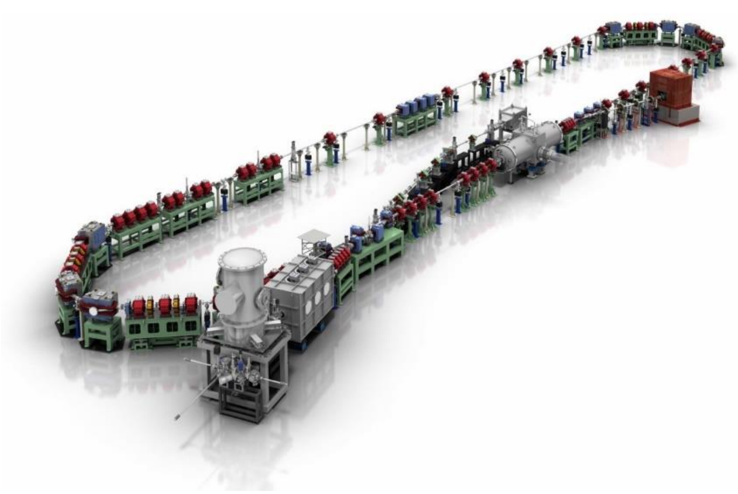
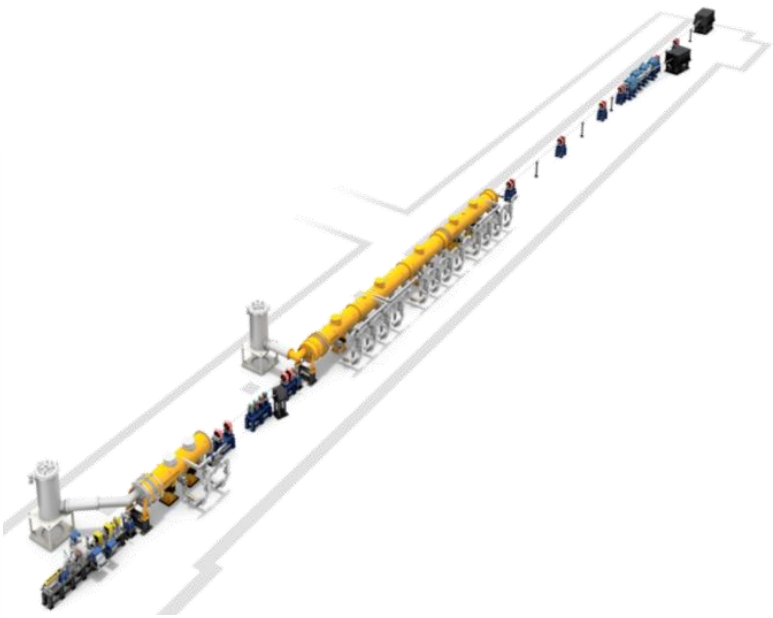
Development of MicroTCA based LLRF control systems at cERL and STF

Feng QIU (KEK) Oct. 18, 2018



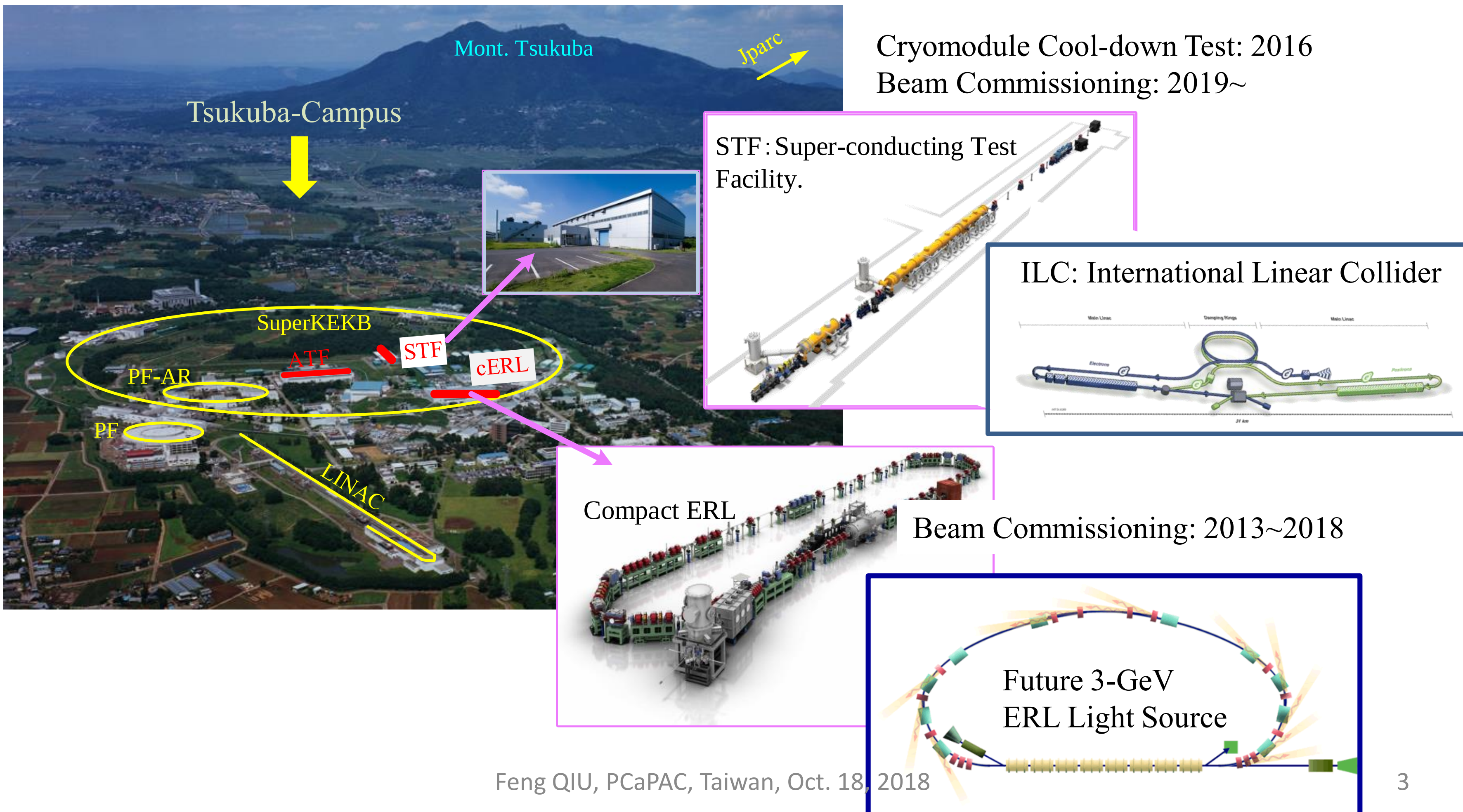


Main Content

- Introduction of cERL and STF facilities
- Development of the μTCA Low Level RF systems
- Performance of the LLRF systems

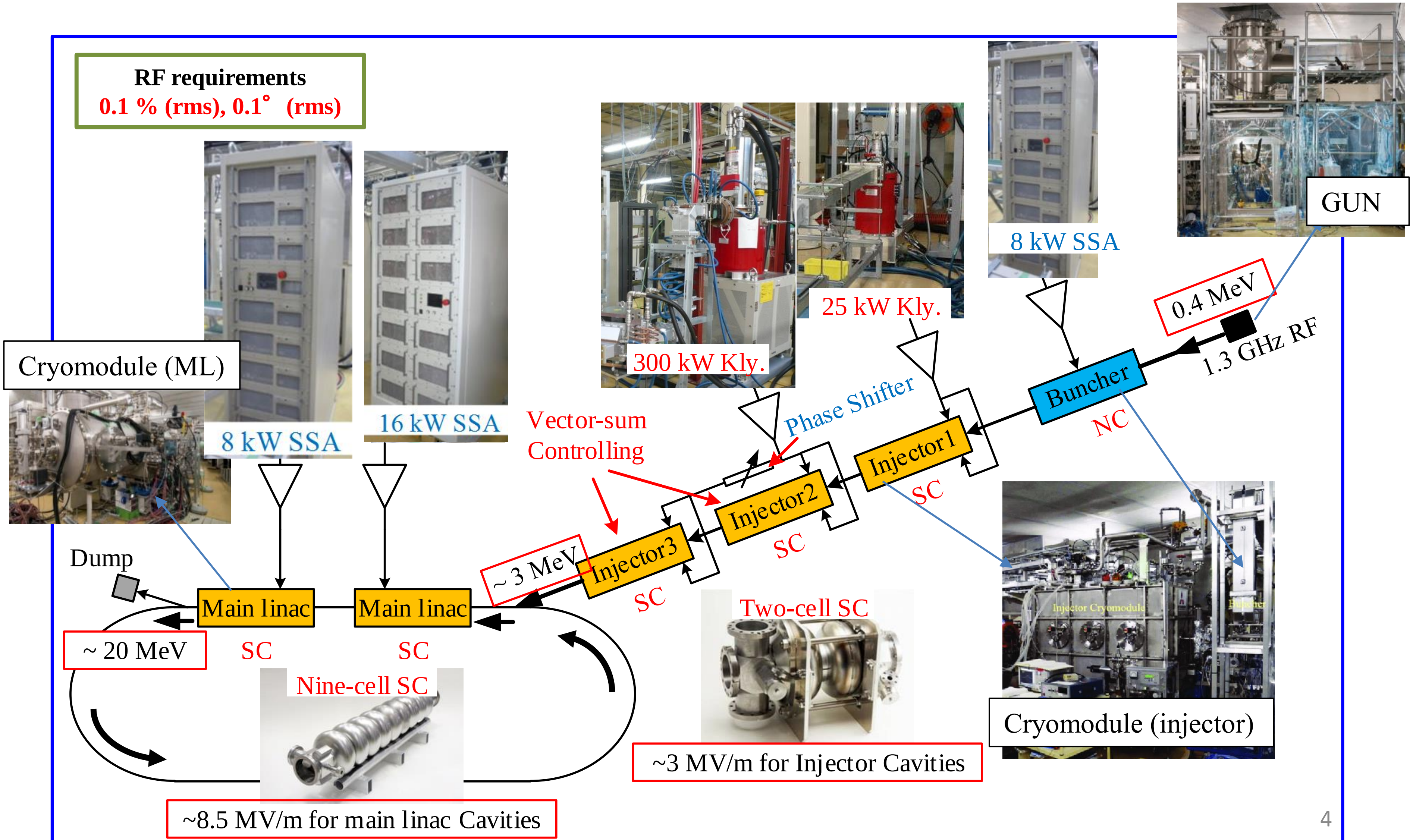
Facilities in KEK

- Compact ERL (cERL): Test facility for 3 GeV light source, 1.3 GHz, Super-conducting (SC) and continuous wave (CW) mode.
- Super-conducting Test Facility (STF): Test facility for ILC, 1.3 GHz, SC and Pulse mode.



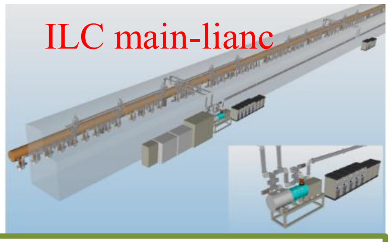
cERL facility

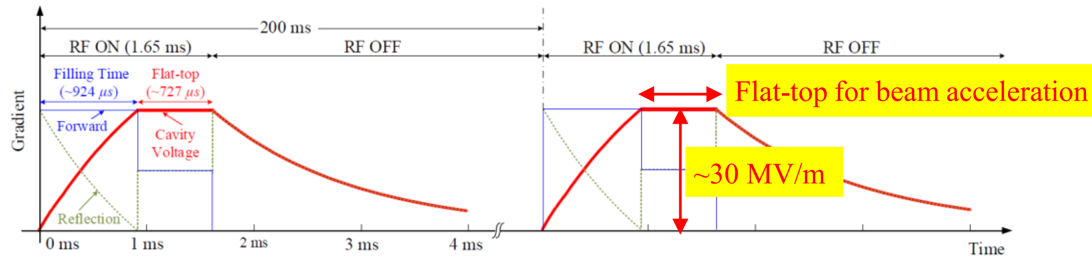
- Injector: 4 cavities (3-SC+1-NC), Mainlinac: 2 SC cavities.
- Various of Power Sources



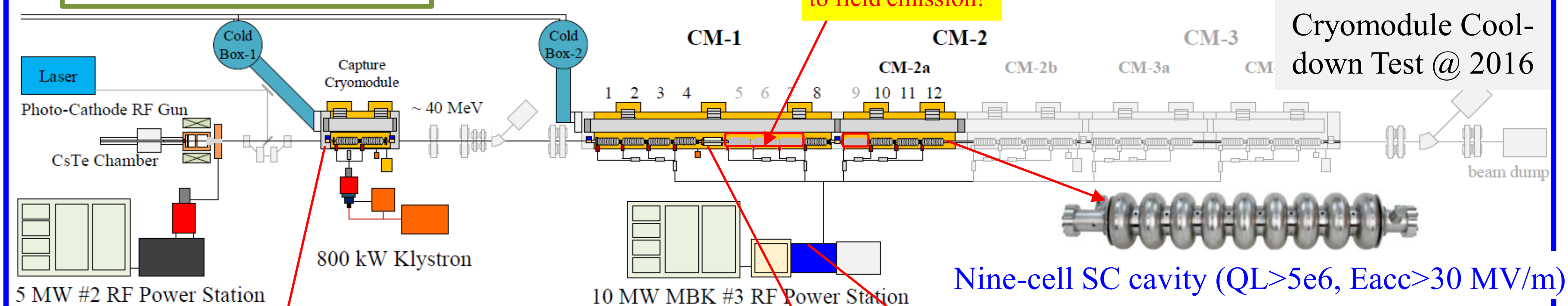
STF facility

- Motivation: Confirmation of the SC cavity technology, and cryomodule fabrication for ILC.
- PS mode (5 Hz, ~1.65 ms). SC nine-cell cavities (QL ≈ 5e6, Eacc about 30 MV/m). Multi-beam klystron (MBK), 10 MW (65%).





RF requirements of ILC
0.07% (rms), 0.35° (rms)



10 MW MBK, (~65%), Toshiba E3736H

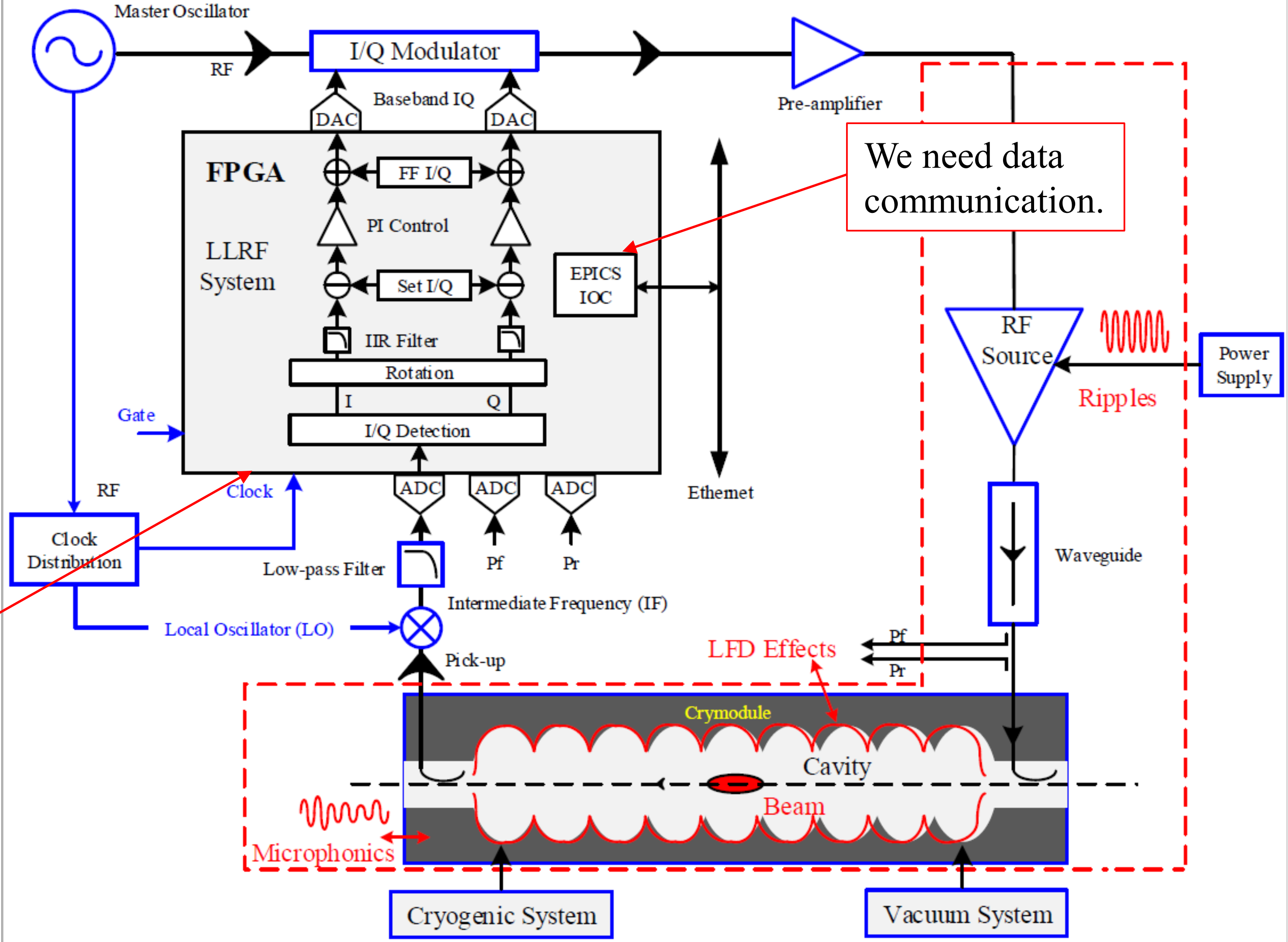
µTCA LLRF systems

Diagram of LLRF system

Why LLRF?

Cavity field is easy to be disturbed

→Need a feedback system to stabilize the cavity field.

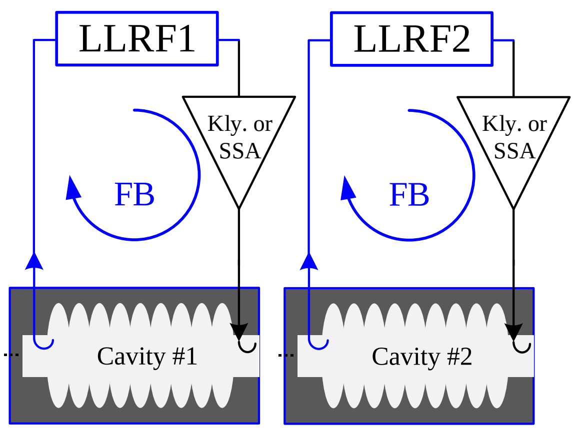


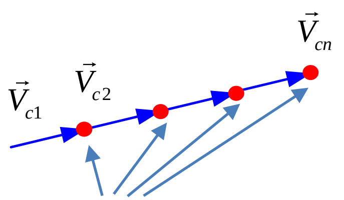
We need an FPGA board to implement the DSP algorithms.

LLRF Systems for cERL and STF

- Individual cavity control (cERL), Vector-sum control (STF).

cERL: One RF source (Kly. or SSA) drives one cavity (except injector2 & 3).



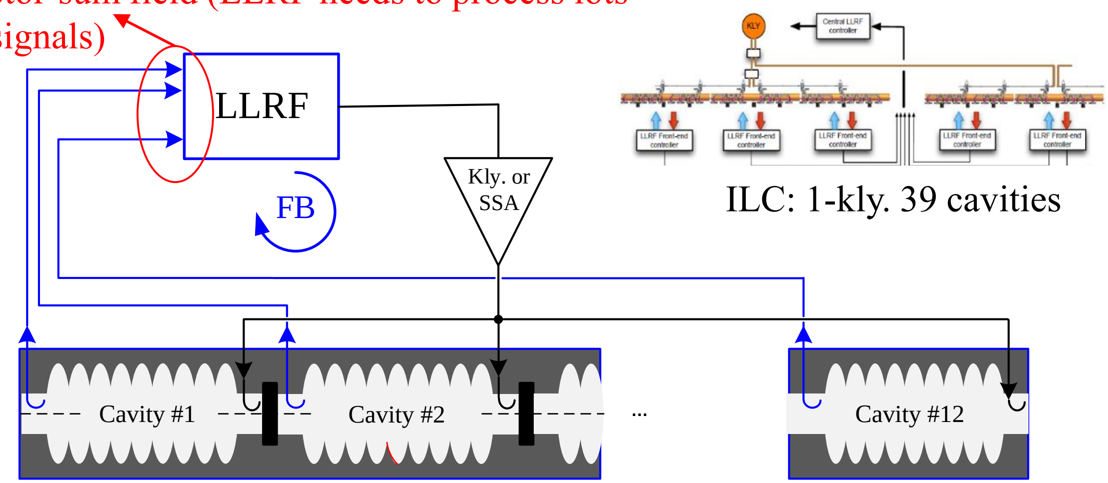


We control every ($\vec{V}_{c1}, \vec{V}_{c2} \cdots \vec{V}_{cn}$)

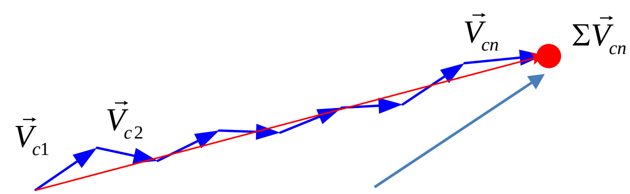
RF requirements
0.1 % (rms), 0.1° (rms)

STF: One RF source drives twelve cavities (actually eight).

Vector-sum field (LLRF needs to process lots of signals)



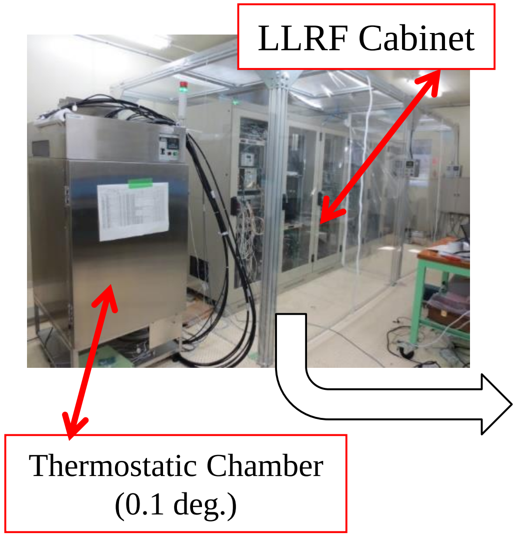
ILC: 1-kly. 39 cavities

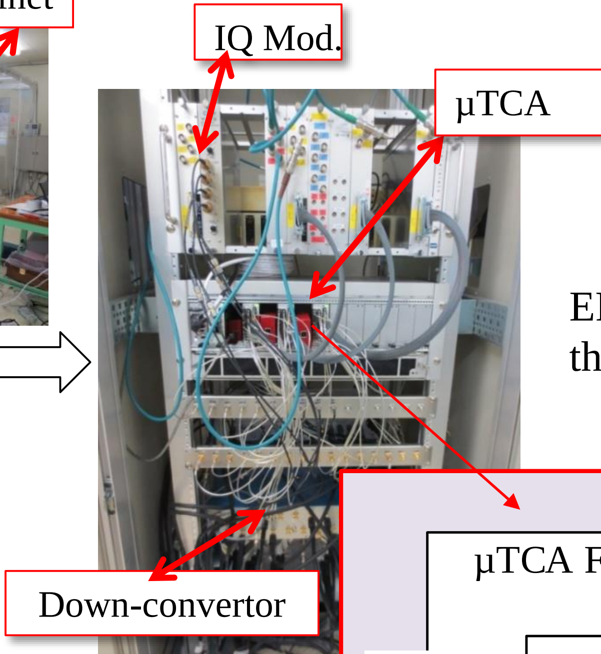


We only control VS ($\Sigma\vec{V}_{cn}$)

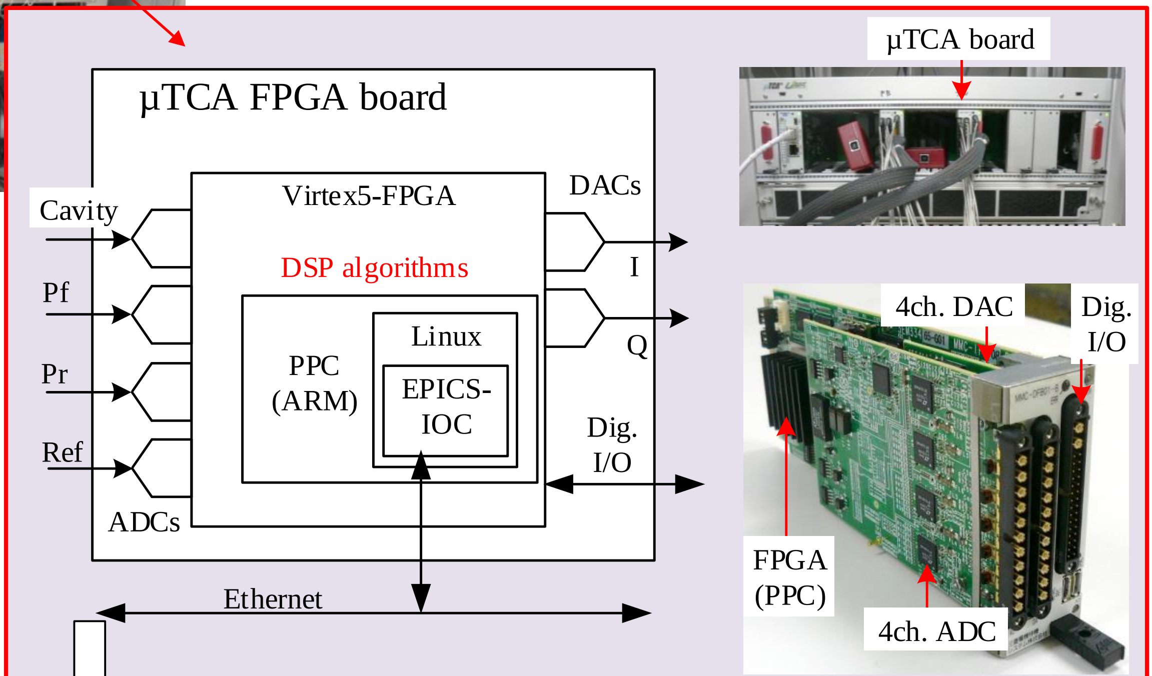
RF requirements of ILC
0.07% (rms), 0.35° (rms)

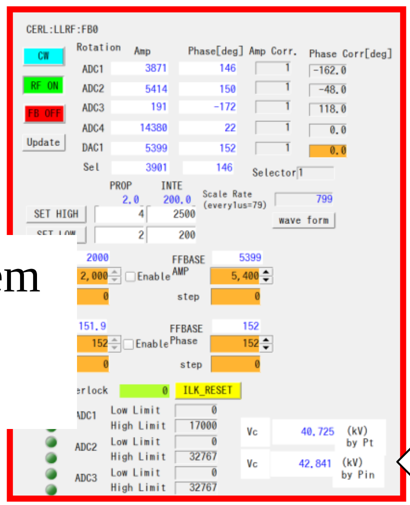
Example: LLRF system @cERL





EPICS is installed inside μTCA and is used as the DAQ (data acquisition) system.

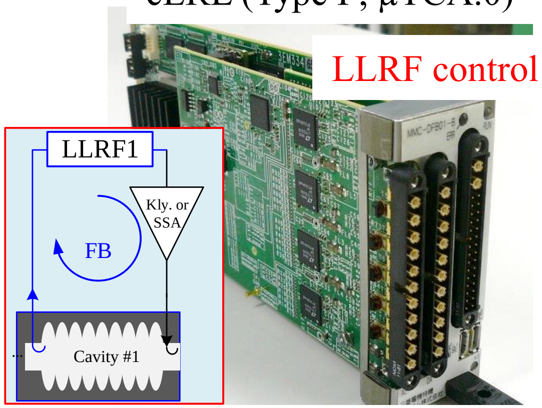




Control System Studio (user interface)

μTCA boards (3 types)

cERL (Type I , μTCA.0)



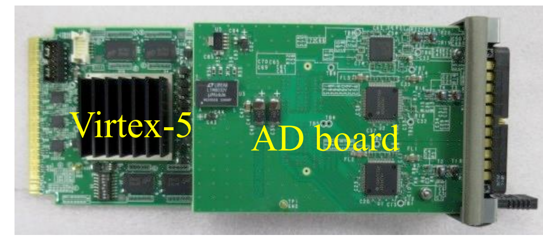
μTCA.0, Virtex-5 FPGA, 4×16-bits ADCs, 4×16-bits DACs

STF (Type II, μTCA.4)

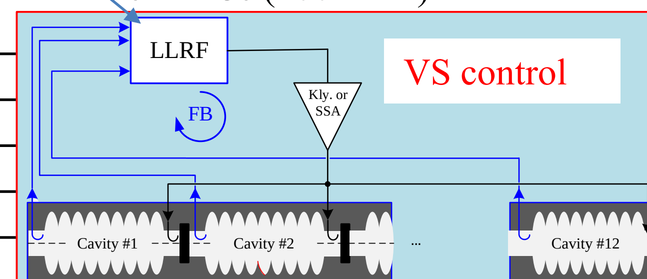
μTCA.4, Zynq-700 FPGA, 12×16-bits ADCs, 2×16-bits DACs

cERL&STF (Type III, μTCA.0)

Monitor the long-term drift (directly sampling)



μTCA.0, Virtex-5 FPGA, 2×14-bits fast ADCs (400 MHz)

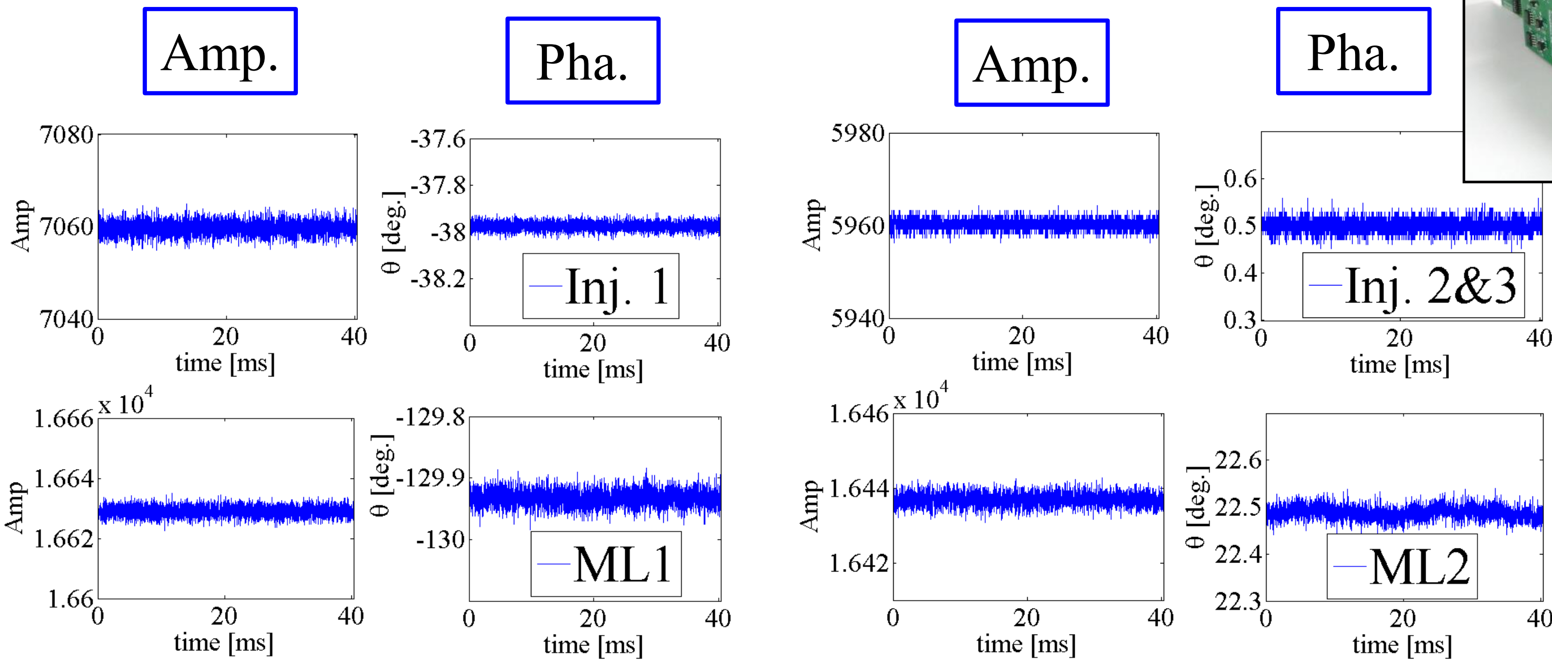


TYPE	TYPE I	TYPE II	TYPE III
Facilities	cERL	STF-II	ERL & STF
Function	LLRF	LLRF	Monitor
Standard	μTCA.0	μTCA.4	μTCA.0
ADC	4×16-bits (LTC2208,130 MSPS)	14×16-bits (AD9650, 105 MSPS)	2×14-bits (ADS5474, 400MSPS)
FPGA	Virtex-5 FX	Virtex-5 FX	Zynq-7000
DAC	4×16-bits (AD9783, 500 MSPS)	2×16-bits (AD9783, 500 MSPS)	N/A
CPU	PPC 440	ARM	PPC 440
OS	Wind River Linux	Xilinx Linux	Wind River Linux

Mitsubishi Electric TOKKI System Co.,Ltd.

Performance of LLRF systems

Performance @ cERL (RF stabilities)

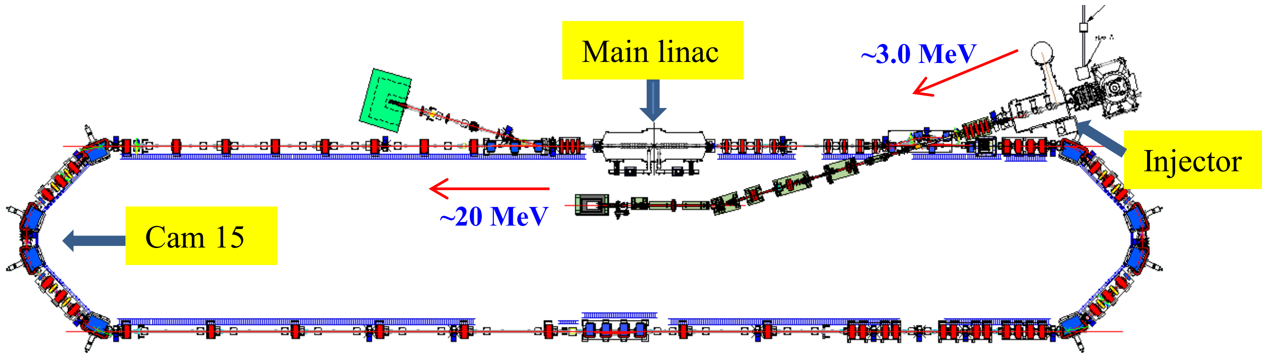


RF stability	Bun.	Inj. 1	Inj. 2&3 (VS)	ML1	ML2	Requirement
ΔA/A [%. rms]	0.07%	0.02%	0.02%	0.01%	0.01%	**0.1%**
Δθ [° .rms]	0.04°	0.02°	0.015°	0.01°	0.01°	**0.1°**

The results need to be confirmed by beam energy stabilities.

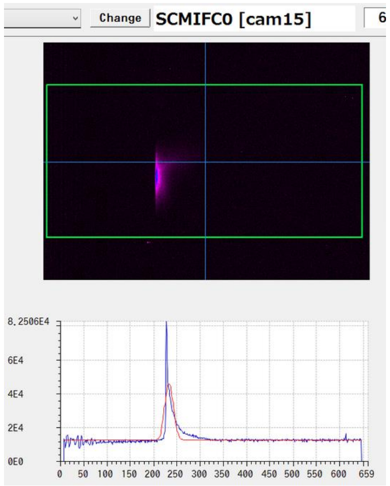
Performance @ cERL (Beam energy)

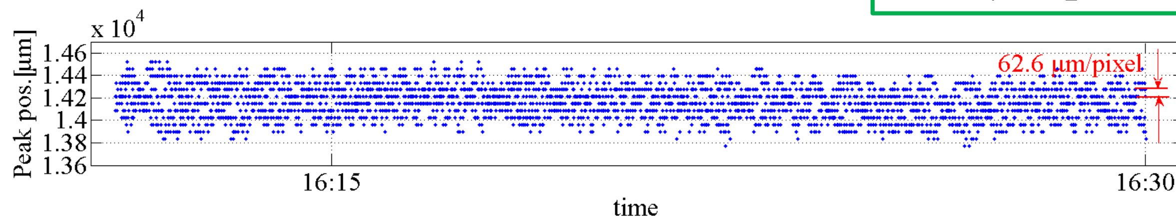
- Beam momentum jitter is measured by screen monitor and determined by the peak point of the projection of the screen.

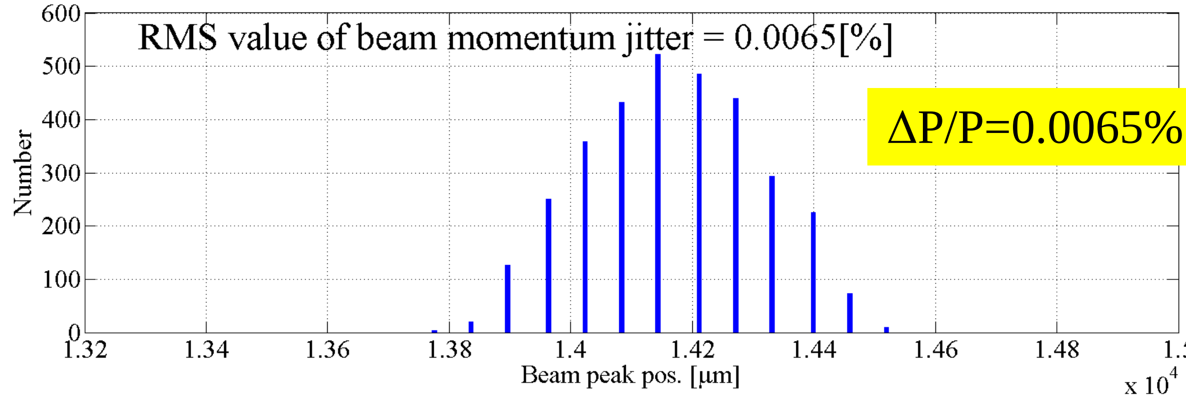


Dispersion
η=2.2m
Resolution
62.6 μm/pixel

Screen monitor

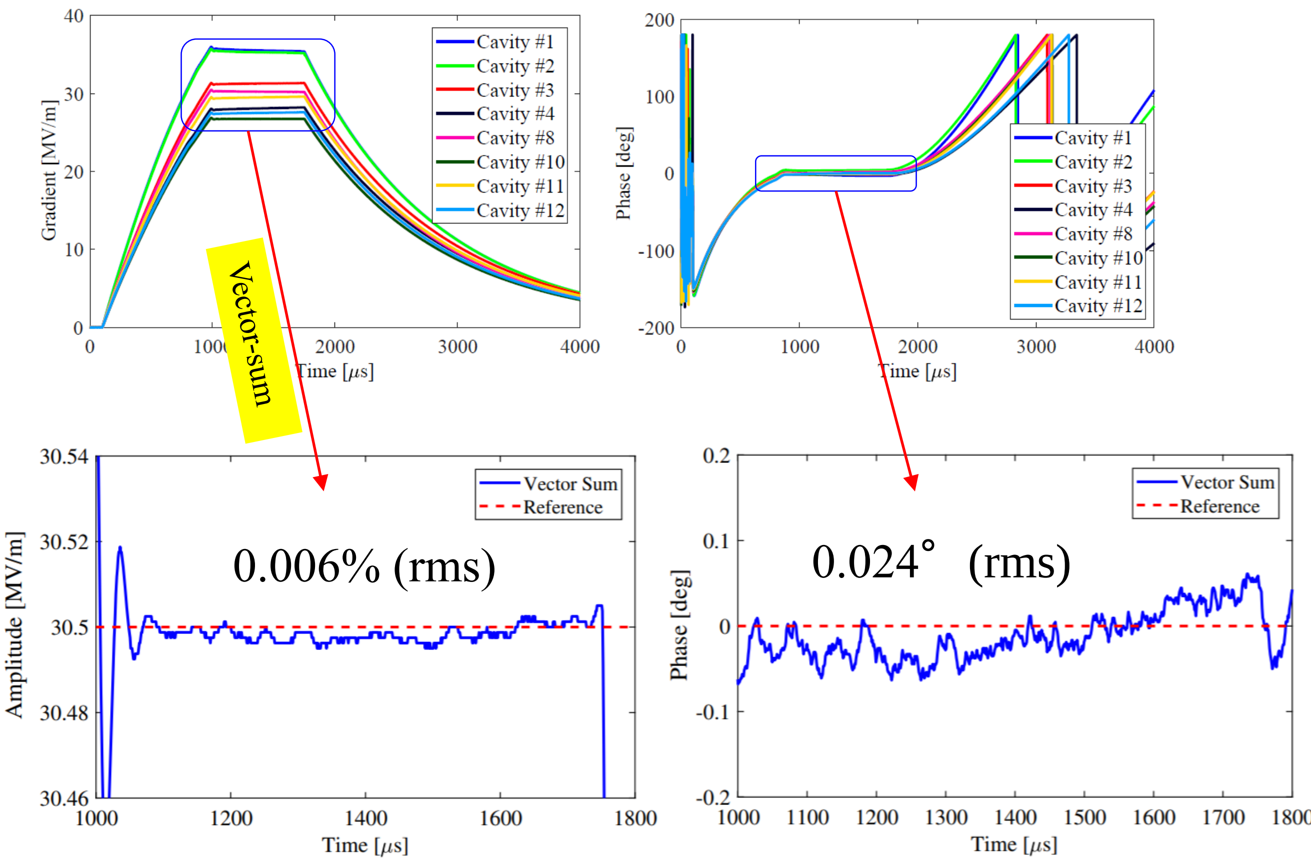


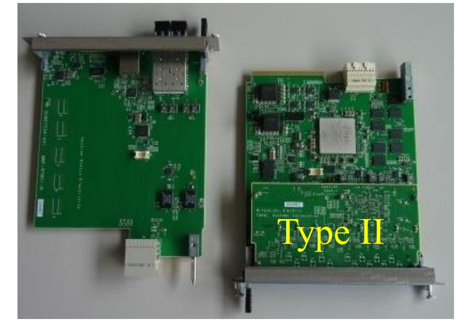




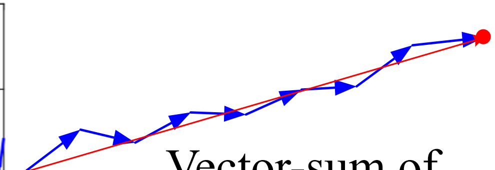
ΔP/P=0.0065%. rms

Performance @ STF (RF Stabilities)





12 ADC channels



Vector-sum of eight cavities

RF stability	Vector-sum (8 cavities)	Requirement
ΔA/A [%. rms]	0.006%	**0.07%**
Δθ [° rms]	0.024°	**0.35°**

Summary

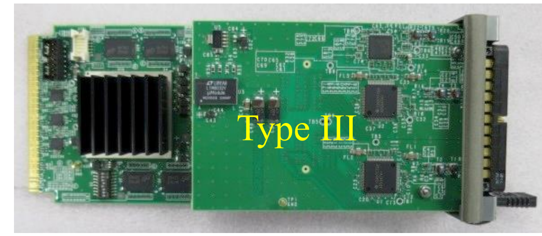
- LLRF control systems with μTCA standards have been developed in cERL and STF.
- Performances satisfied our requirements.

Thank you for your attention

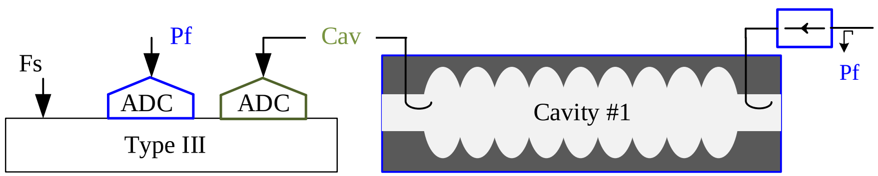
Back up

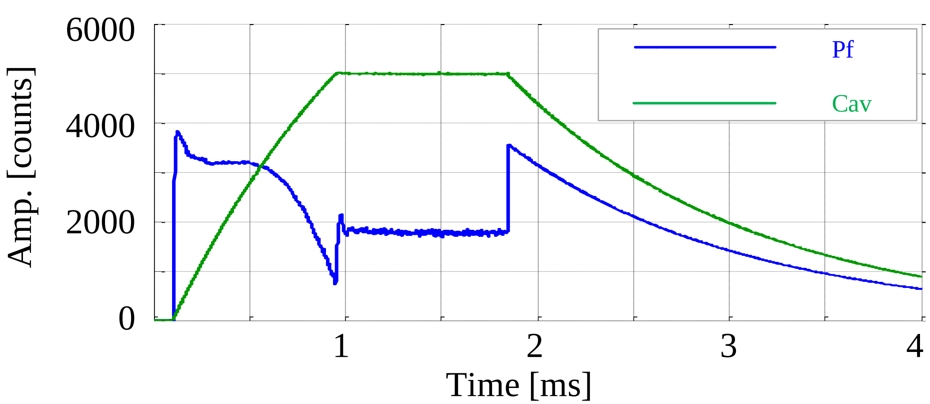
Performance @ STF (Directly Sampling)

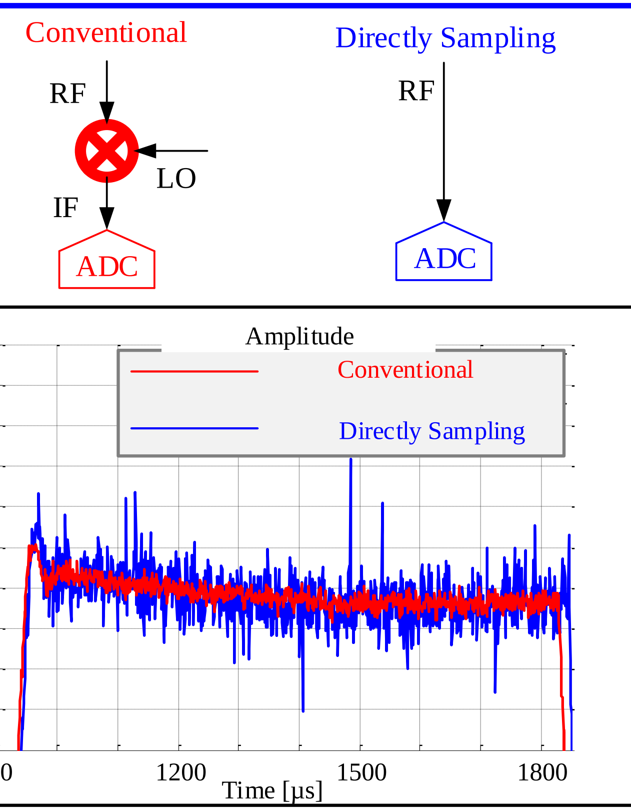
- Stabilities becomes worse (directly sampling).
- Monitor the long-term drift of the master oscillator and local oscillator (we can use digital filter to improve the precision).



Fast ADC: 400 MHz



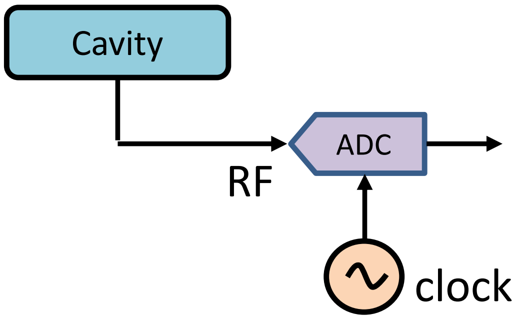


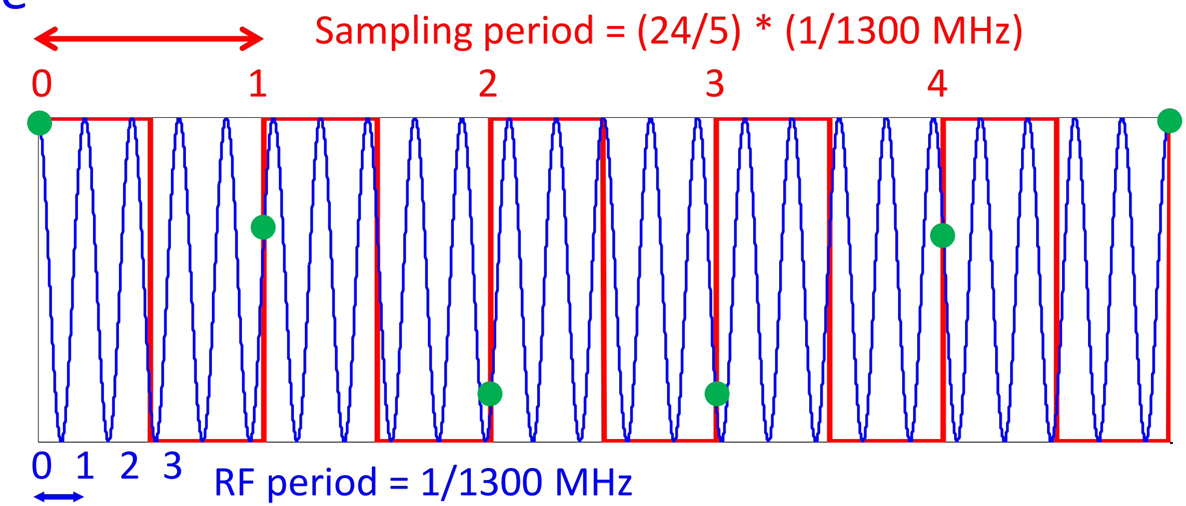


0.1% (rms) and 0.1° (rms)

Direct Sampling Method

- Under-sampling procedure for Direct Sampling:





- The relation of f_{clock}, f_{RF} and I,Q components:

$$f_{clock} = \frac{L}{N} \cdot f_{RF}$$

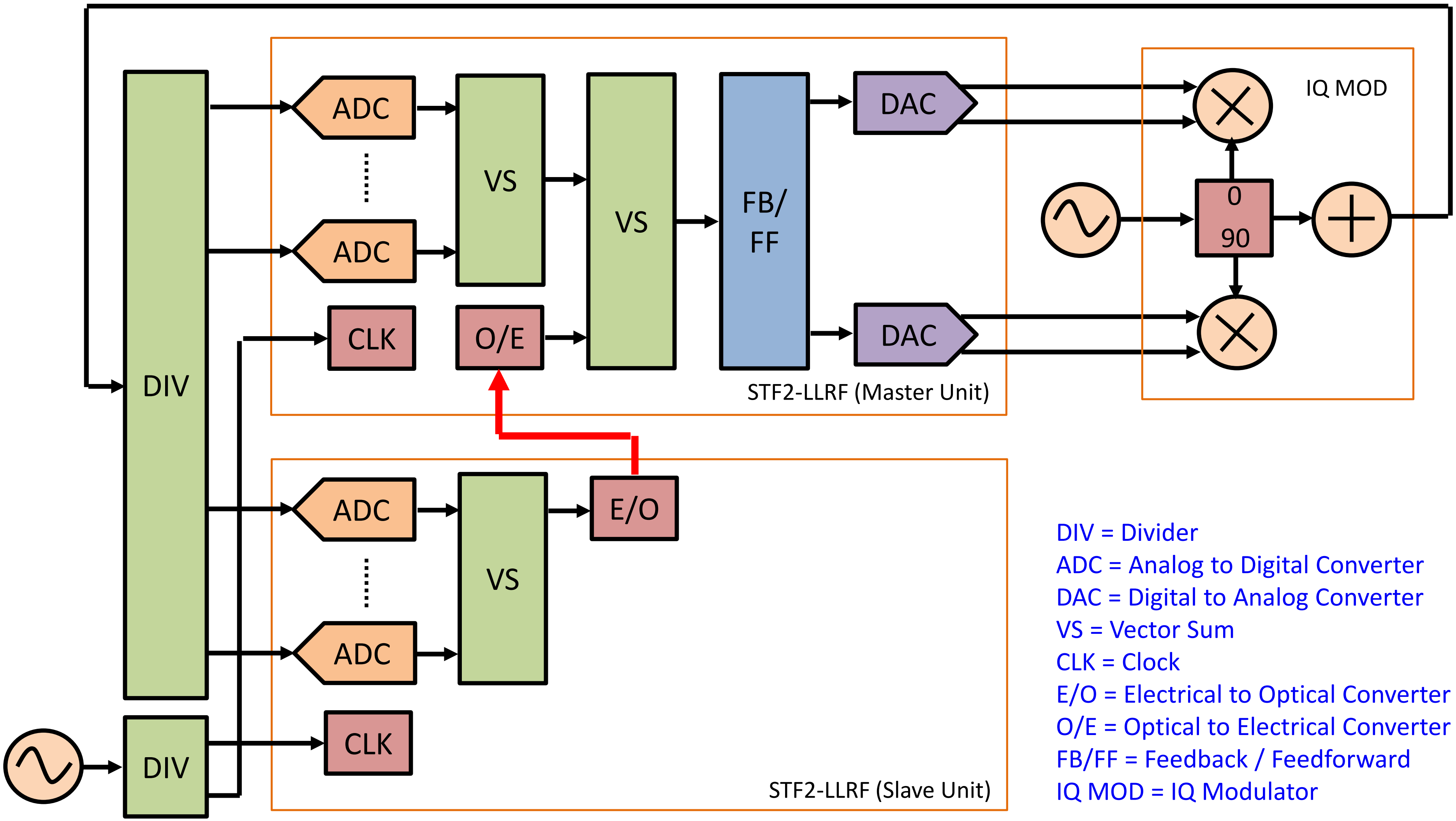
$$I = \frac{2}{L} \sum_{k=1}^{L} V_{RF}(k) \cdot \cos\left(2\pi \frac{N}{L} \cdot k\right)$$

$$Q = \frac{2}{L} \sum_{k=1}^{L} V_{RF}(k) \cdot \sin\left(2\pi \frac{N}{L} \cdot k\right)$$

f_{RF} = 1300 MHz

No	L Data Cycle	N RF Period	clock [MHz]
1	5	24	270.83
2	4	19	273.68
3	3	14	278.57
4	6	29	268.97
5	7	29	313.79

Optical Communication Test Bench in STF, KEK.



DIV = Divider
ADC = Analog to Digital Converter
DAC = Digital to Analog Converter
VS = Vector Sum
CLK = Clock
E/O = Electrical to Optical Converter
O/E = Optical to Electrical Converter
FB/FF = Feedback / Feedforward
IQ MOD = IQ Modulator