DEVELOPMENT PROGRESS OF THE 4TH GENERATION OF SWITCHING POWER SUPPLY FOR CIRCULAR INDUCTION ACCELERATORS

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Abstract

A novel synchrotron called an induction synchrotron (IS) was developed at KEK in 2006. In the IS, charged particles are accelerated and confined by bipolar high-voltage pulses generated by switching power supply (SPS), which is one of the key technologies for IS. In this work, the 4th generation of SPS, based on full-bridge circuit with 3.3 kV high-speed MOSFET is developed. Compared with previous prototype, better waveforms have been achieved since the structure has been redesigned with a better balance of parasitic inductance and capacitance in each arm. The heat dissipation performance at high frequency has been improved through applying MOSFETs in parallel, and confirmed by single shot test and 50 kHz test. Temperature at 500 kHz has been also estimated by simulation.

BACKGROUND

KEK digital accelerator (KEK-DA) [1-3] is the first circular induction accelerator [4] in the world, which utilizes induction cells instead of RF cells to accelerate particle bunches. Essentially, the induction cell is a one-to-one pulse transformer, of which the particle bunch is the secondary coil. The induction cell accelerates particle bunches that are passing by, just like the RF cell does in a synchrotron. The induction cell is driven by switching power supply (SPS) directly, without any waveguide. So it has no frequency bandwidth limitation compared with RF cell. Therefore, the circular induction accelerator, either Synchrotron or Microtron, can works without an injector.

As the heart of circular induction accelerator, SPS generates positive pulses to drive the induction cells, while negative pulses to reset the magnetic core. Up to now, 3 generations of switching power supplies have been developed. The voltage rating of the Si-MOSFET of the 1st generation [5] is only 1.0 kV, so 7 MOSFETs in series were needed for each arm. Years later, 1.2 and 2.4 kV SiC-JFET were utilized for the 2nd [6-8] and 3rd [9, 10] generation respectively. In recent years, the 4th generation, which utilized 3.3 kV SiC-MOSFET, was under development [11]. After heat dissipation analysis and structure redesign [12], the updated 4th generation of SPS has been manufactured and tested in this work.

UPDATED DESIGN AND MANUFACTURE

The 4th generation of SPS is based on full-bridge circuit with 3.3 kV high-speed MOSFETs. Bipolar high-voltage pulses are generated within an operation period. On the load, positive pulse is generated when ARM 1 and 4 are on but ARM 2 and 3 are off, while negative pulse is generated when ARM 2 and 3 are on but ARM 1 and 4 are off.

Some problems emerged in the previous design of the 4th generation of SPS, as seen in Fig. 1. Firstly, each ARM contained only one MOSFET. The switching loss of the MOSFETs was high and heat dissipation was serious. Secondly, buses are made of wide copper plate and stacked together, with isolating paper sandwiched between them. The parasitic capacitance of buses inevitably increased the rise-time and fall-time of the output pulse. Thirdly, parasitic capacitance of buses was unbalanced because of its asymmetric structure. The V_{ds} of each MOSFET was not half of HV before switching on and could not return to half of HV after switching off, unless an extra equalizing CR circuit was applied.

The problems mentioned above have been improved in the updated design, as seen in Fig. 2. Two parallel MOSFETs have been applied in each ARM, to reduce the

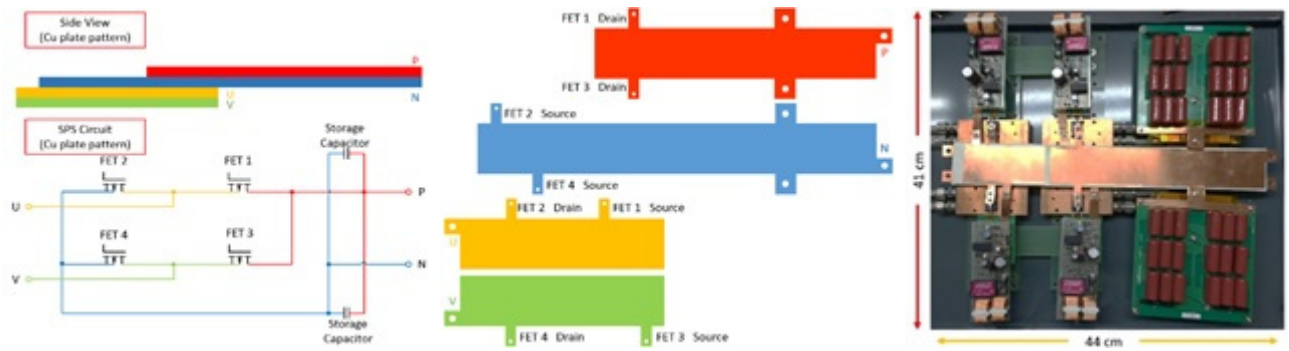

Figure 1: Circuit schematics, structure of buses and picture of the previous design of 4th generation of SPS.

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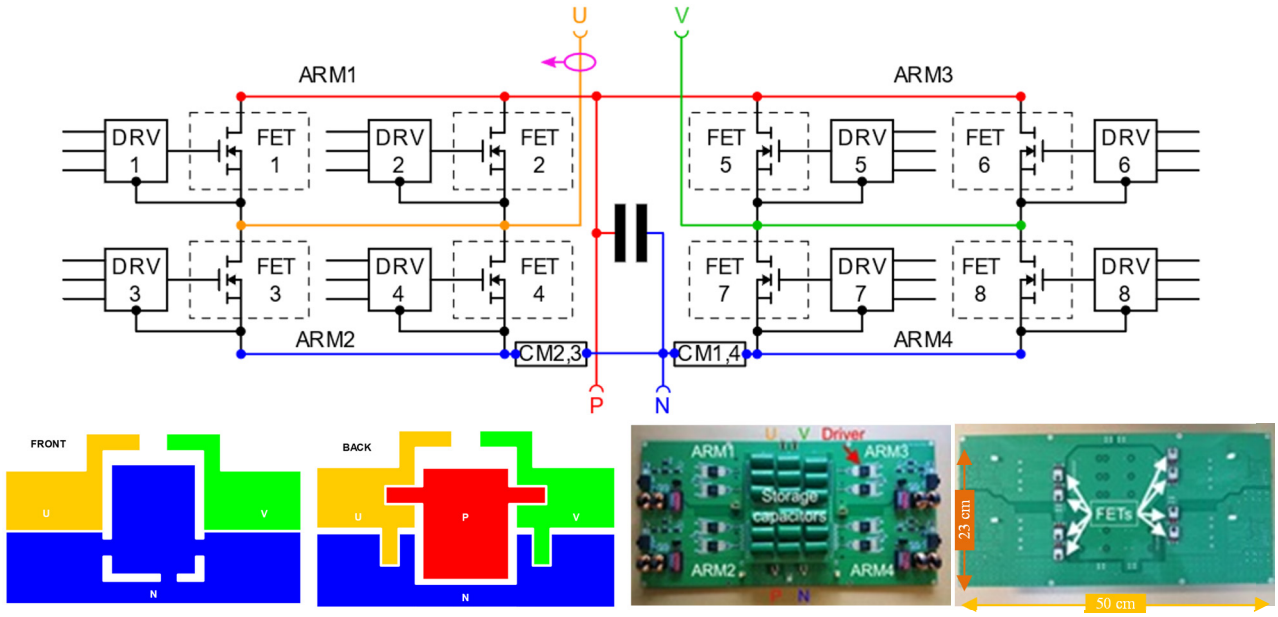

Figure 2: Circuit schematics, structure of buses and picture of the updated design of 4th generation of SPS.

switching loss. The buses have been redesigned. The parasitic capacitance of UV reaches almost 0. The parasitic capacitance of UN, VN, UP and VP has been reduced as low as possible and is almost the same. Thus, the rise-time and fall-time of the output pulse have been kept low, and the equalizations of output voltage and V_{ds} of ARMs have been achieved. The details of the experiment results are described in the next Section.

SINGLE SHOT PERFORMANCE

Waveforms and switching loss

A single shot test of the updated manufactured 4th generation of SPS was conducted with an 80 Ω resistive load. The pulse width was set as 300 ns and the delay time between positive and negative pulses was set as 500 ns. The V_{ds} of each ARM was measured one by one, by using a pair of HV differential probes. The current of load, which was approximated as the current of each ARM (I_{ds}), was measured by a current transformer at the same time. Figure 3 shows the V_{ds} waveform, I_{ds} waveform, switching power (P_{sw}) and switching loss (E_{loss}) of ARM 1 as an example, at a HV varying from 0.5 kV to 2.5 kV. P_{sw} was calculated by V_{ds} and I_{ds} waveforms ($P_{sw} = V_{ds} I_{ds}$) and the E_{loss} was the integration of P_{sw} ($\int V_{\mathrm{ds}} I_{\mathrm{ds}} dt$). The waveforms of V_{ds} were improved significantly, compared with the previous design. Because of the fairly low and balanced parasitic capacitance of buses, V_{ds} of each ARM was half of HV before switching on and returned to half of HV after switching off as expected. The I_{ds} was around 31 A and the fall-time of V_{ds} of each ARM was around 25 ns at 2.5 kV HV and 80 Ω load.

Figure 4 (a) shows the switch-on loss, switch-off loss and total switching loss of each ARM. The total switching loss increased more at higher HV. Switch-on loss was defined as the device loss generated from off state to the time point of drain voltage falling to 10% of the DC value in the switch-on period. Switch-off loss was defined as the device loss generated from the time point of drain voltage rising from 10% to 100% of the recovery voltage in the switch-off period. The switch-off loss was higher than the switch-on loss, because the rise-time of V_{ds} was longer than the

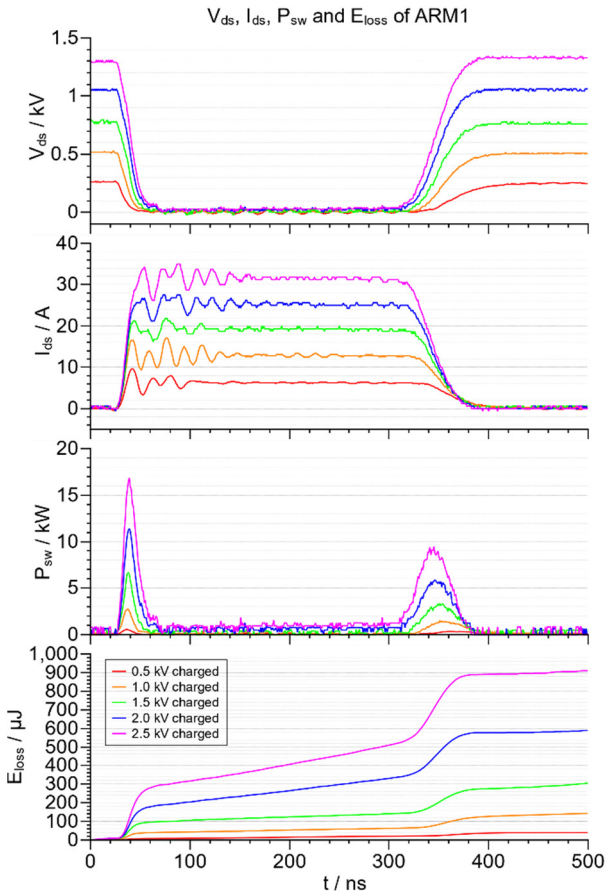

Figure 3: V_{ds} waveform, I_{ds} waveform, P_{sw} and E_{loss} of ARM 1.

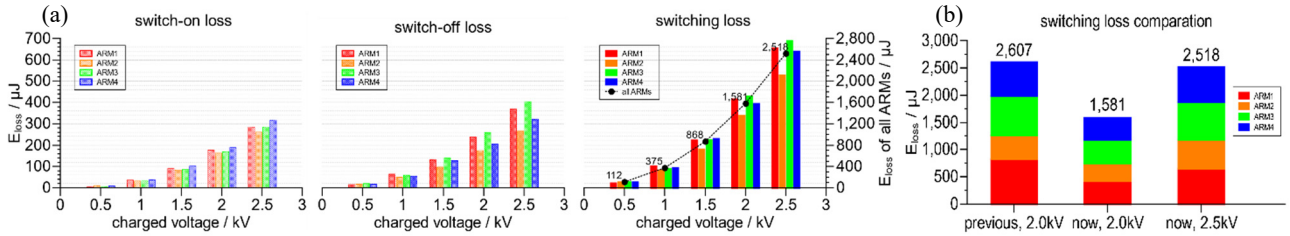

Figure 4: (a) Switch-on loss, switch-off loss and total switching loss of each ARM at different HV. (b) Switching loss comparation of the previous and the updated SPS.

fall-time of V_{ds}. Note that the parasitic capacitance of UV was almost zero, the time constant, which was determined by the product of the capacitance and resistance of the load, was ensured as low as possible. So the fall-time and rise-time of V_{ds} in this test could furthest reflect the MOSFET characteristics.

As seen in Fig. 4 (b), in the same condition (2 kV HV, 80 Ω load), compared with the previous design, the total switching loss has been reduced from 2607 μJ to 1581μJ. Almost 40% improvement on the previous design has been achieved. Furthermore, at 2.5 kV HV the total switching loss is 2518 μJ.

Current monitor calibration

In the updated design, two 0.1 Ω sampling resistors were in series with ARM2 and 4 respectively. Their voltage was extracted by coaxial cables with matching resistors to the oscilloscope. Then the sampling resistor could be used as a current monitor (CM) to measure the conducting current of ARMs and monitor the operation state. A calibration test was executed, in which the measurement results from current transformer (CT) were treated as standard value. The calibration factor should be 20 theoretically. In our test, the calibration factors were 22 and 21 for these current monitors respectively as seen in Fig. 5. On the other hand, high-frequency oscillations were observed as noise signal in the waveform. A low-pass FFT filtering process was applied at 35 MHz, which was determined by an empirical formula $f = 0.35/t_{fall}$, where t_{fall} was 10 ns to 25 ns in our experiment. The results were shown in Fig. 6. The solid line waveforms were from current transformer (CT), while the

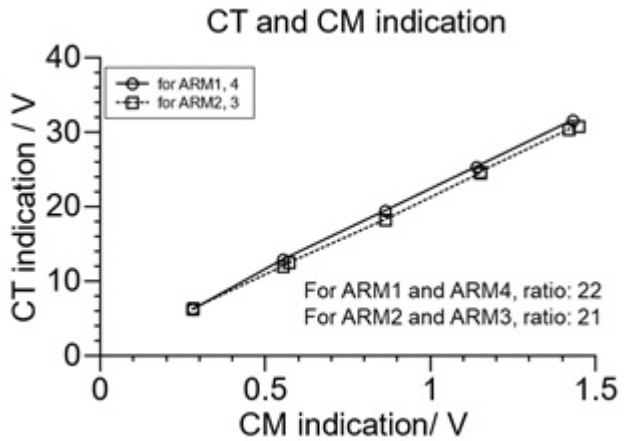

Figure 5: The indications from current transformer and current monitors.

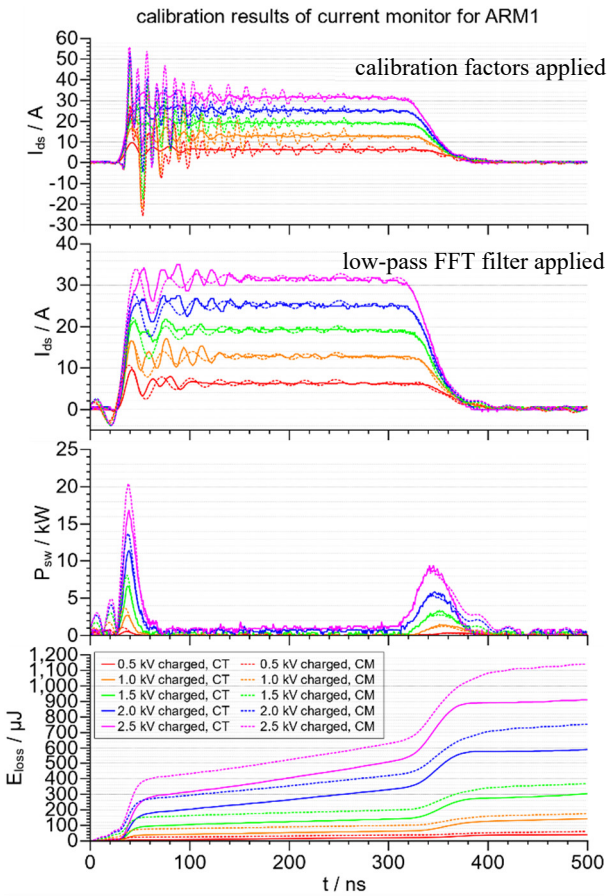

Figure 6: Comparation of the standard waveforms from current transformer and the processed waveforms from current monitor.

dot line waveforms were from current monitor (CM). In the top graph, only calibration factor was applied. In the second graph, the low-pass FFT filtering process was added. The waveforms from CT and CM became almost the same. The third and bottom graph shows the calculated P_{sw} and E_{loss}. The value from CM was a little higher than that from CT, because the rise-time and fall-time were slightly longer, which were caused by the resistance and inductance of the sampling resistor inevitably.

CONTINUOUS OPERATION

A low frequency continuous operation test was conducted successfully with an 80 Ω resistance load, 2.5 kV HV and 50 kHz. As seen in the Fig. 7, the output voltage of the load was almost the same as that in a single shot test.

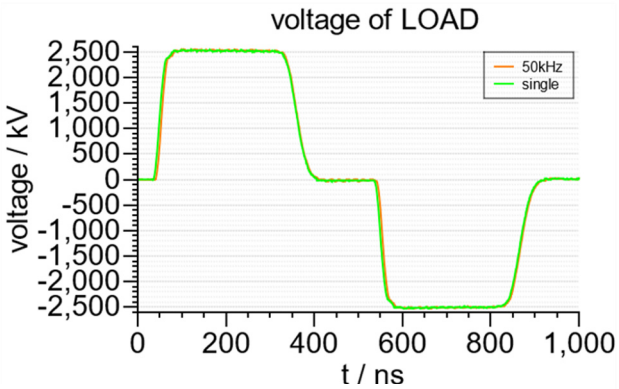

Figure 7: Output voltage of the load at 50 kHz and single shot.

Thanks to the updated design, the heat power of the MOSFET was around 17.5 W (50 kHz) and the temperature increment of the cases of two randomly selected MOSFETs were 5.9 °C and 6.8 °C respectively. A heat dissipation simulation based on multi-physics and finite element method, in which the model had been confirmed previously, was carried out. As seen in Table 1, the results of experiment and simulation matched well. Furthermore, if the SPS operate at 500 kHz, the estimated heat power of each MOSFET would be 175 W. According to the simulation, the junction temperature would be as high as around 120 °C, but still lower than the rated value 175 °C. So, the MOSFETs` survivability of the updated SPS was optimistic at the condition of 500 kHz, 2.5 kV, 31 A and double 300 ns pulse.

Table 1: Heat Dissipation in Experiment and Simulation

Settings	**Experiment**	**Simulation**	
Air temperature	≈22 °C	22 °C	
Water temperature	26.3 °C	26 °C	
TIM	≈0.1 mm Indium	0.1 mm Indium	
Water flow / L/min	≈ 0.75	0.75	
Frequency / kHz	50	50	500
Heat power / W	≈ 17.5	17.5	175
Results			
ΔT of cases / °C	5.9 & 6.8	5.2 & 5.4	17.7 & 20.7
ΔT of water / °C	0.5	0.6	6.6
Junction temperature /°C	-	35.3 & 35.5	119 & 121

CONCLUSION

The 4th generation of Switching Power Supply for Circular Induction Accelerators is redesigned and manufactured. The heat dissipation and output waveform are improved by parallel MOSFETs and new structure respectively. A current monitor component is applied and calibrated. Stable 50 kHz operation is achieved, and the junction temperature of MOSFET at up to 500 kHz is estimated and the result is optimistic.

ACKNOWLEDGEMENTS

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