Overview of SINAP Timing System

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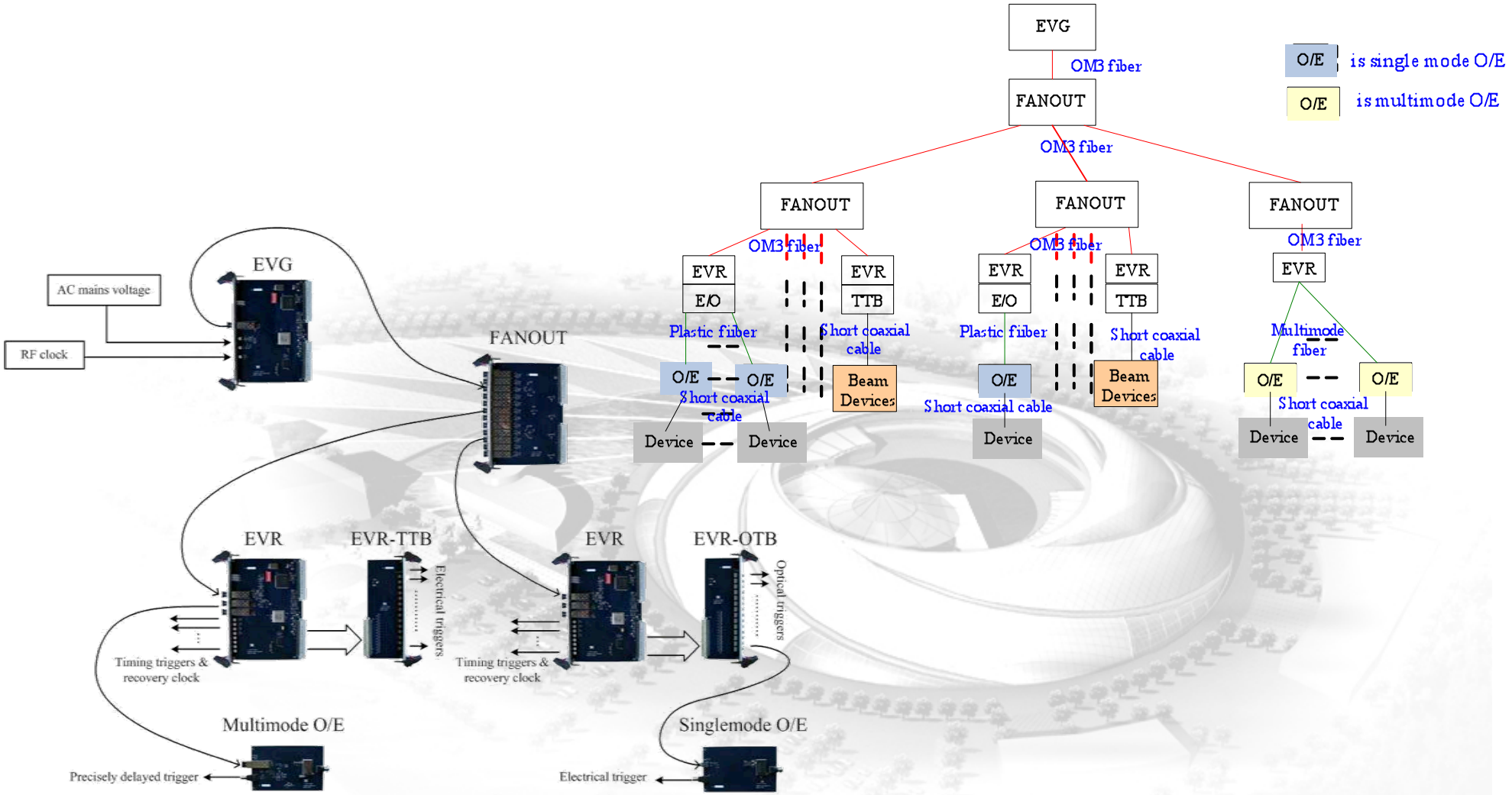
Outline

- v1 timing system structure
- v1 hardware
- v1 performance
- v1 in PLS-II
- v2 timing system structure
- v2 hardware

SINAP v1 timing system structure



Hardware List

- SINAP v1 timing system:
  - EVG
  - EVR
  - FANOUT
  - TTL VME Transition Board
  - Plastic fiber VME Transition Board
  - Multimode fiber O/E
  - Plastic fiber O/E

EVG

VME 6U module; A16D32 addressing

Input: 1ch RF clock (0 – 10 dBm)

1ch AC line (3Vp-p typical)

Output: 1ch multi-mode fiber

1ch Sequence RAM trigger (TTL)

EVR

VME 6U module; A16D32 addressing

Input: 1ch multi-mode fiber

1ch interlock input (TTL)

Output: 3ch TTL trigger/clock

3ch LVPECL trigger/clock

1ch CML RF recovery clock

2ch Multi-mode fiber trigger

FANOUT

VME 6U module

Input : 1ch multimode fiber

Output: 12ch multimode fiber

TTL VME Transition Board

VME transition board

Output: 14ch TTL trigger

Plastic Fiber VME Transition Board

VME transition board;

Output: 14ch optic trigger

(Agilent HFBR-1528)

Multi-mode Fiber O/E

Standalone module

Input: 1ch multi-mode fiber

1ch power supply (24V/1A)

Output: 1ch TTL (50ohm)

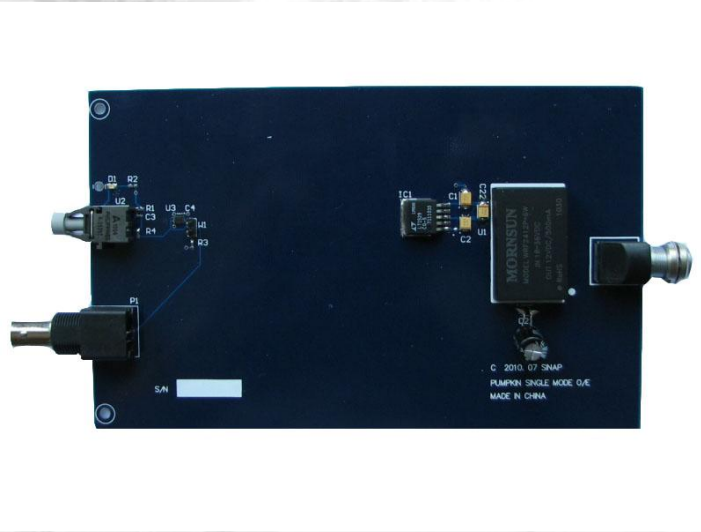
Plastic Fiber O/E

Standalone module

Input: 1ch multi-mode fiber

1ch power supply (24V/1A)

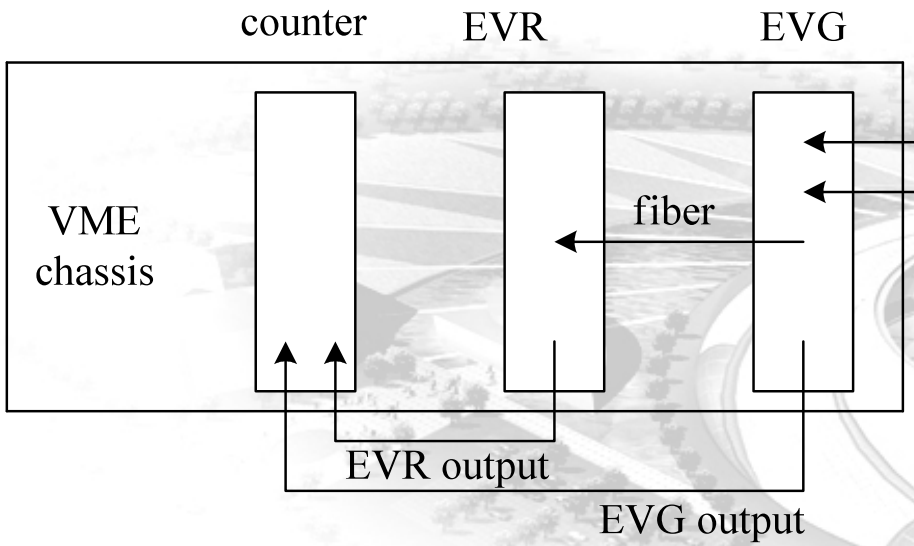
Output: 1ch TTL

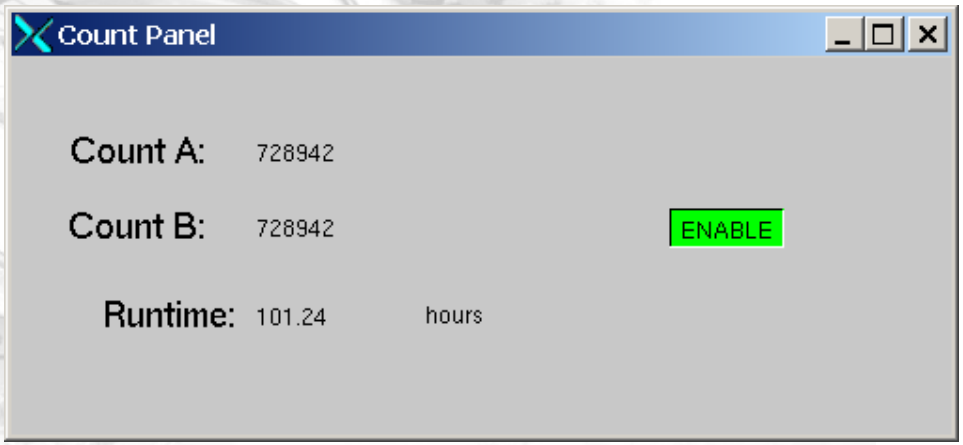


Performance Testing

- Stability

coding-decoding error



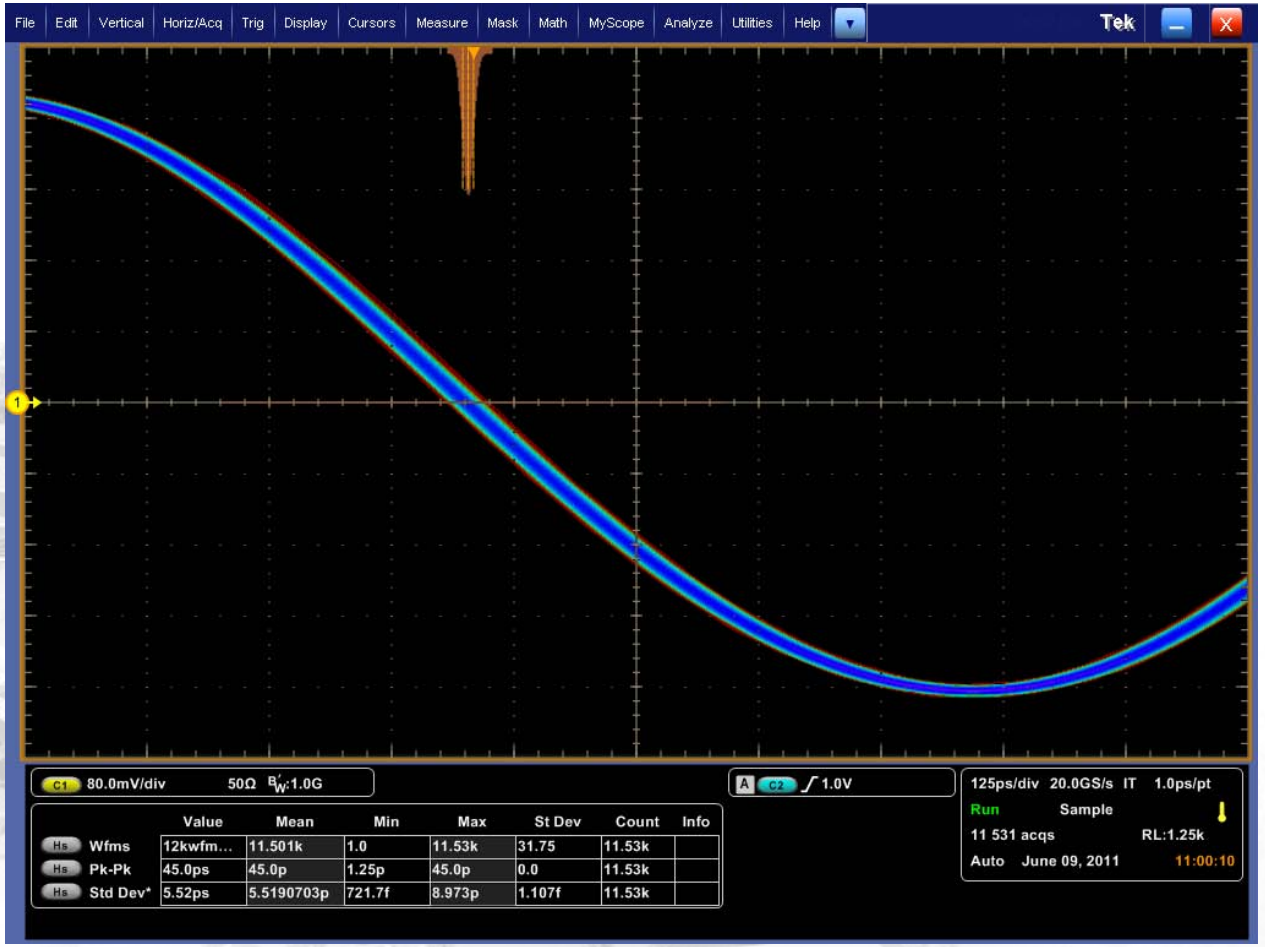


Performance Testing

- Jitter

EVR TTL output

< 6ps

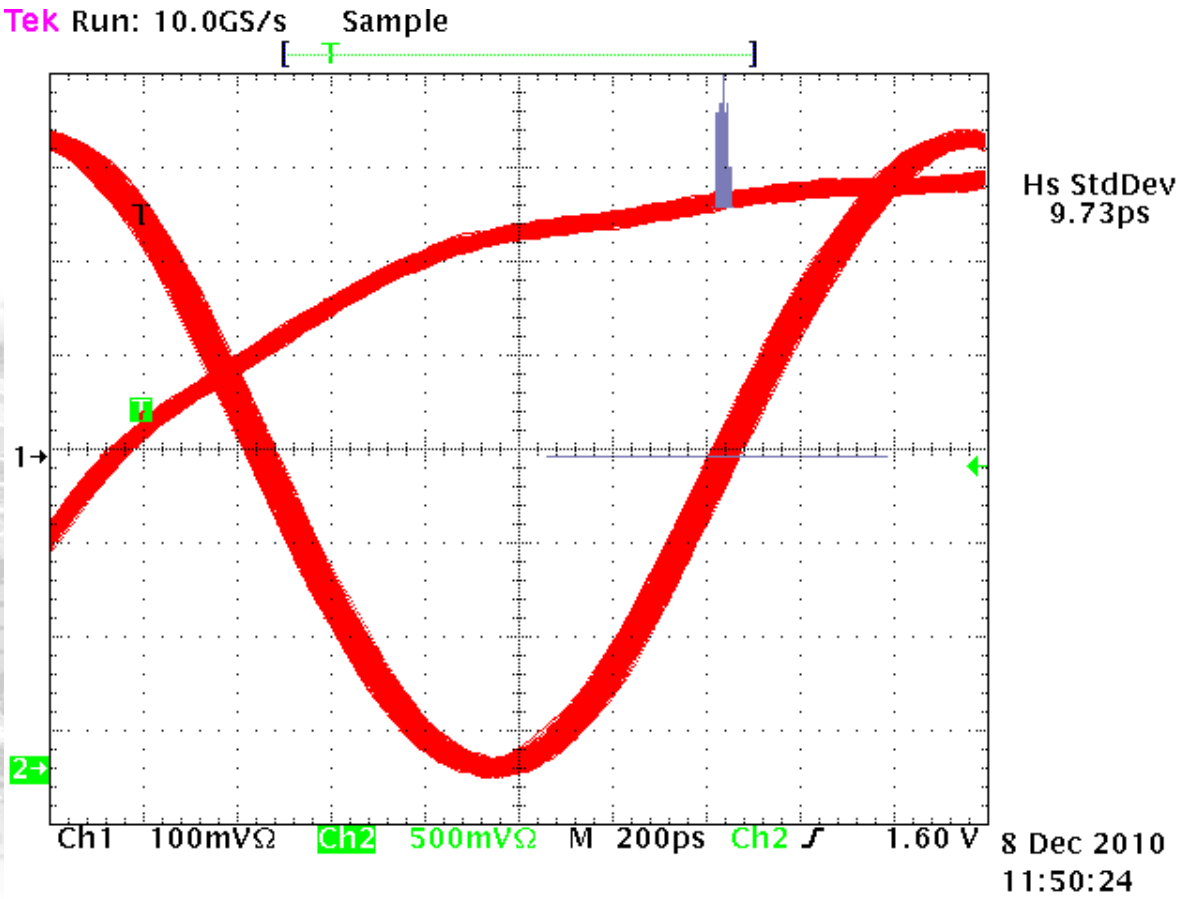


Performance Testing

- Jitter

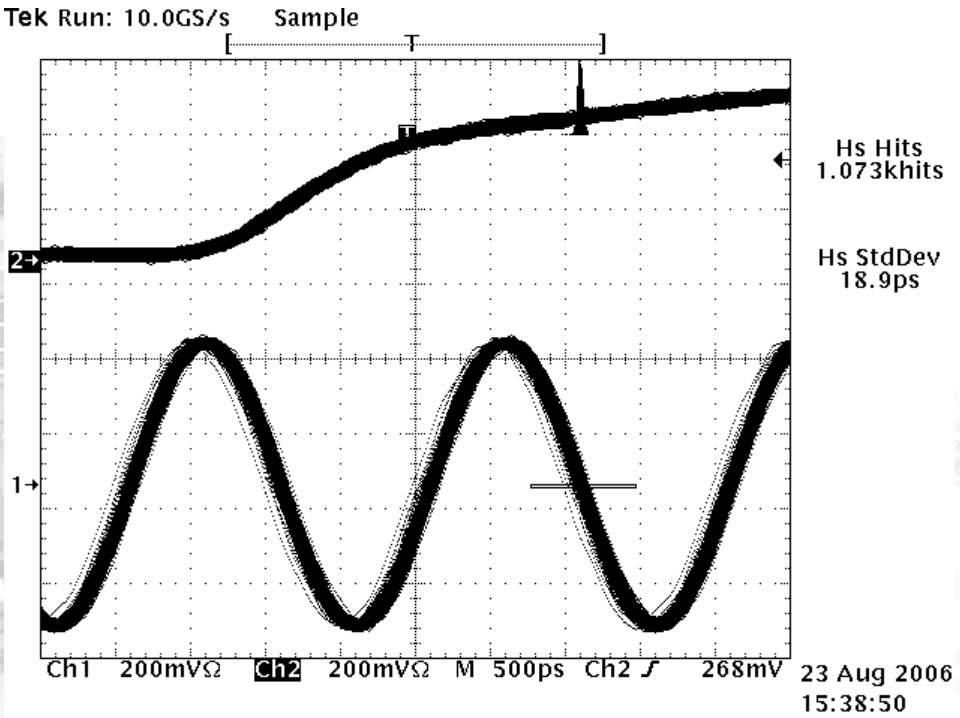
Multi-mode O/E output

< 10ps



MRF Jitter Performance

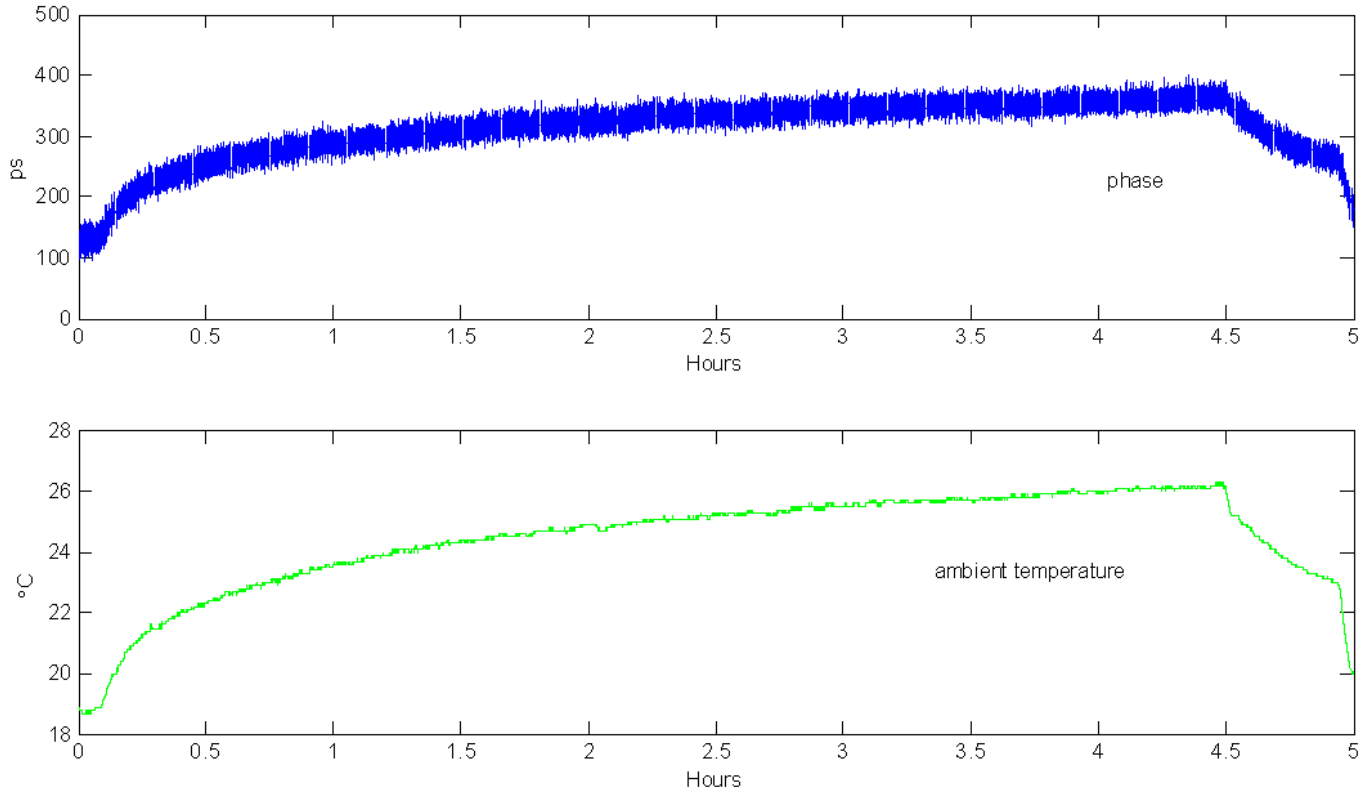
- EVR TTL output > 18ps



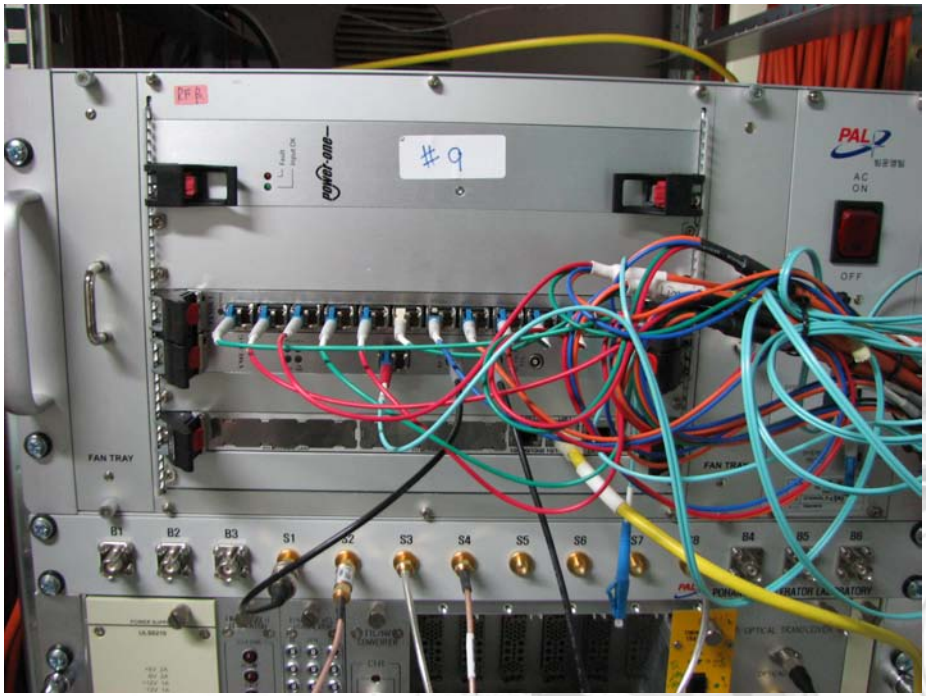
Performance Testing

- Phase Shift

Phase shift with temperature changing (35ps/℃)

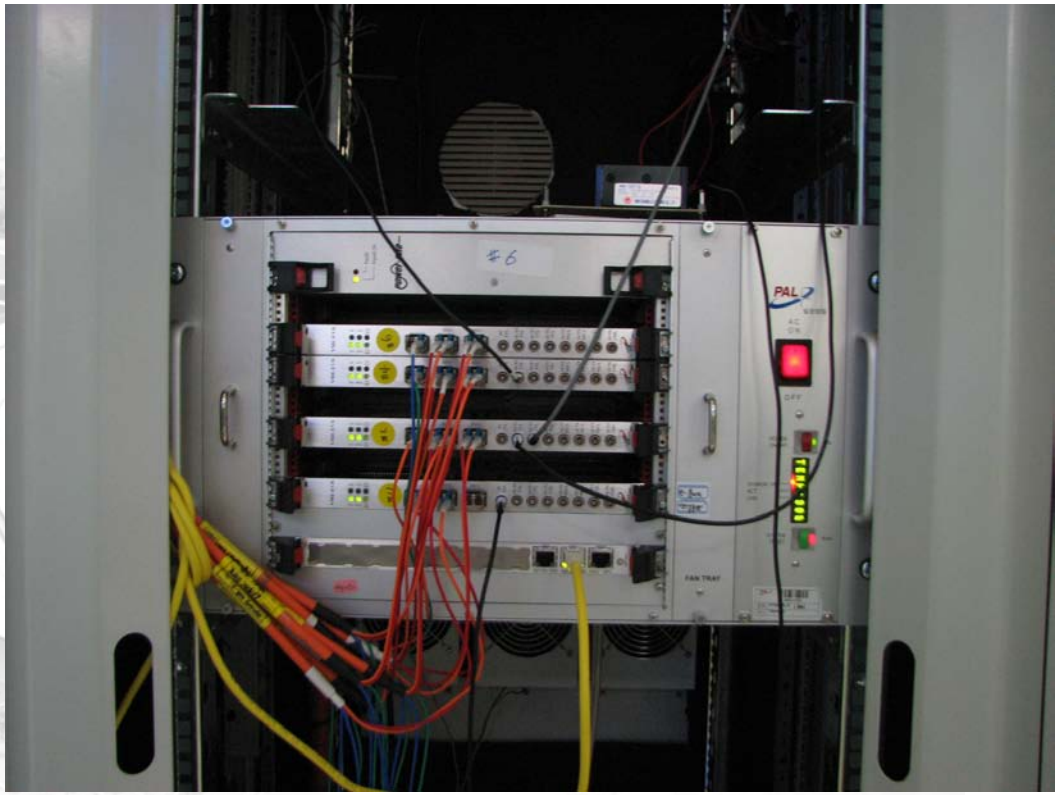


v1 in PLS-II

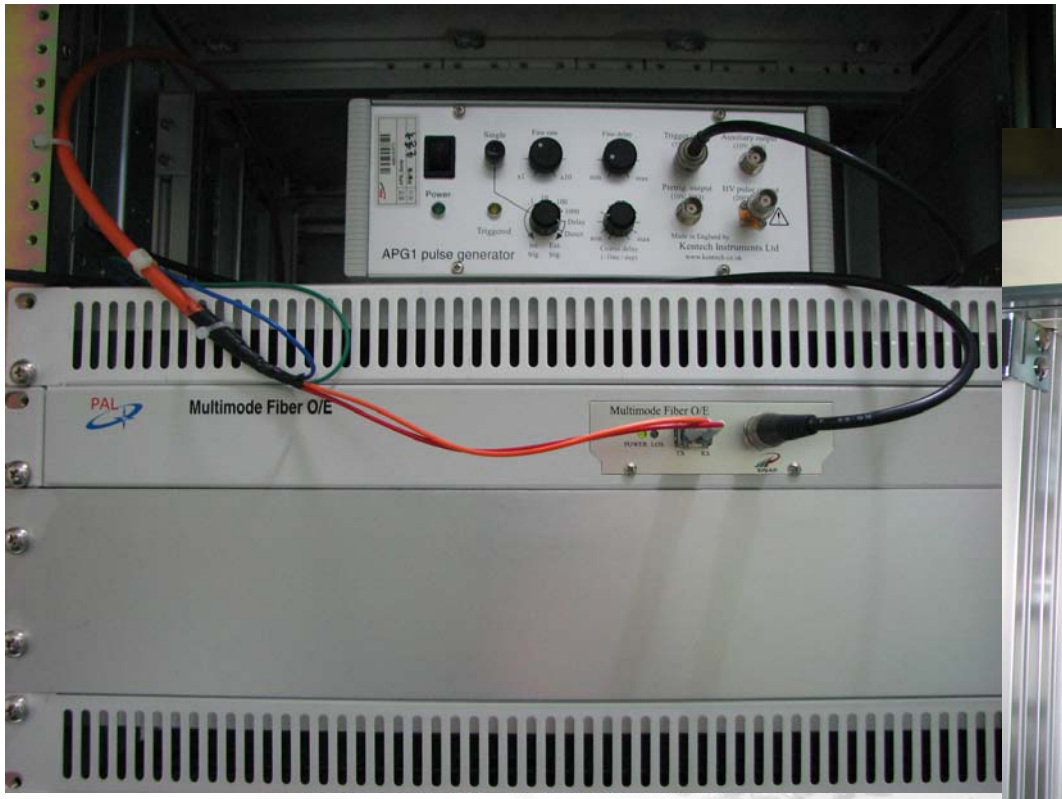


in RF station (EVG)

in LINAC control room



v1 in PLS-II

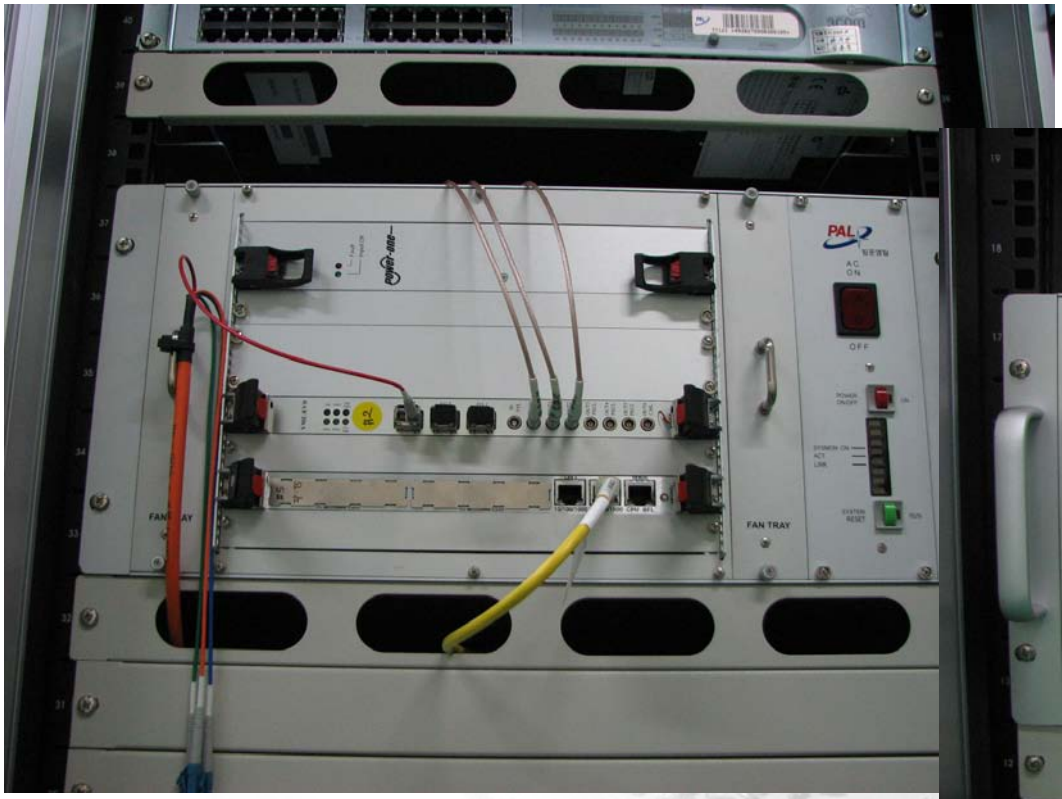


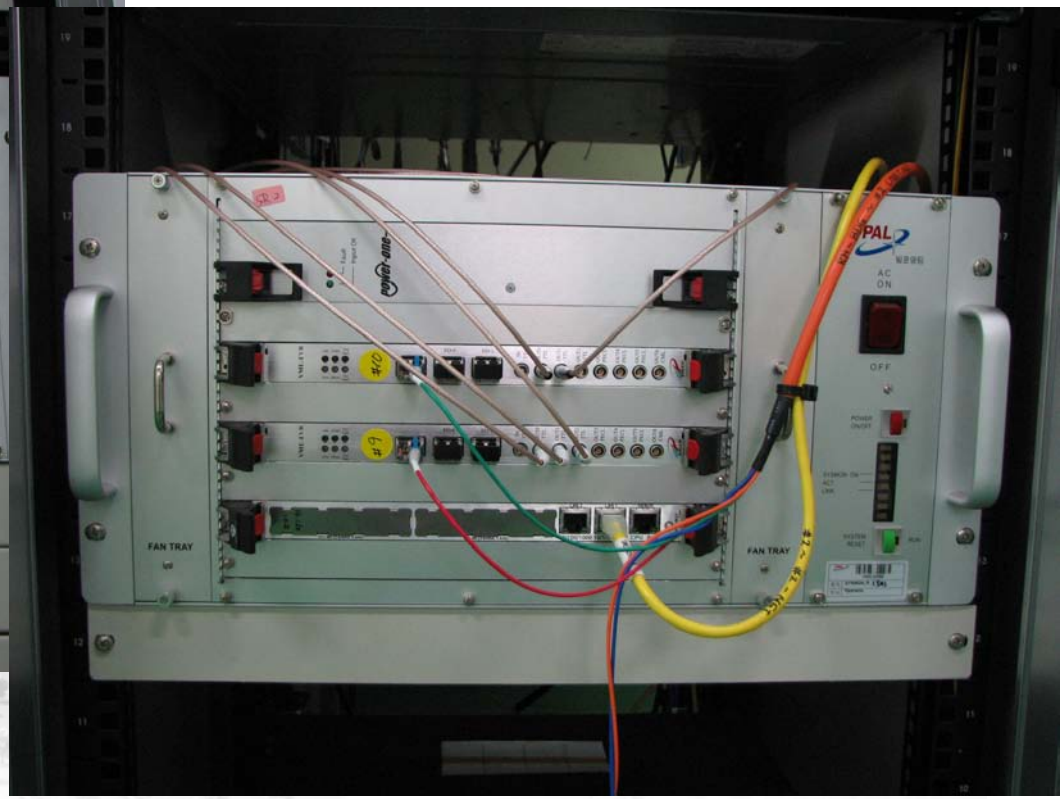
in E-gun

in Klystron & Modulator

V1 in PLS-II

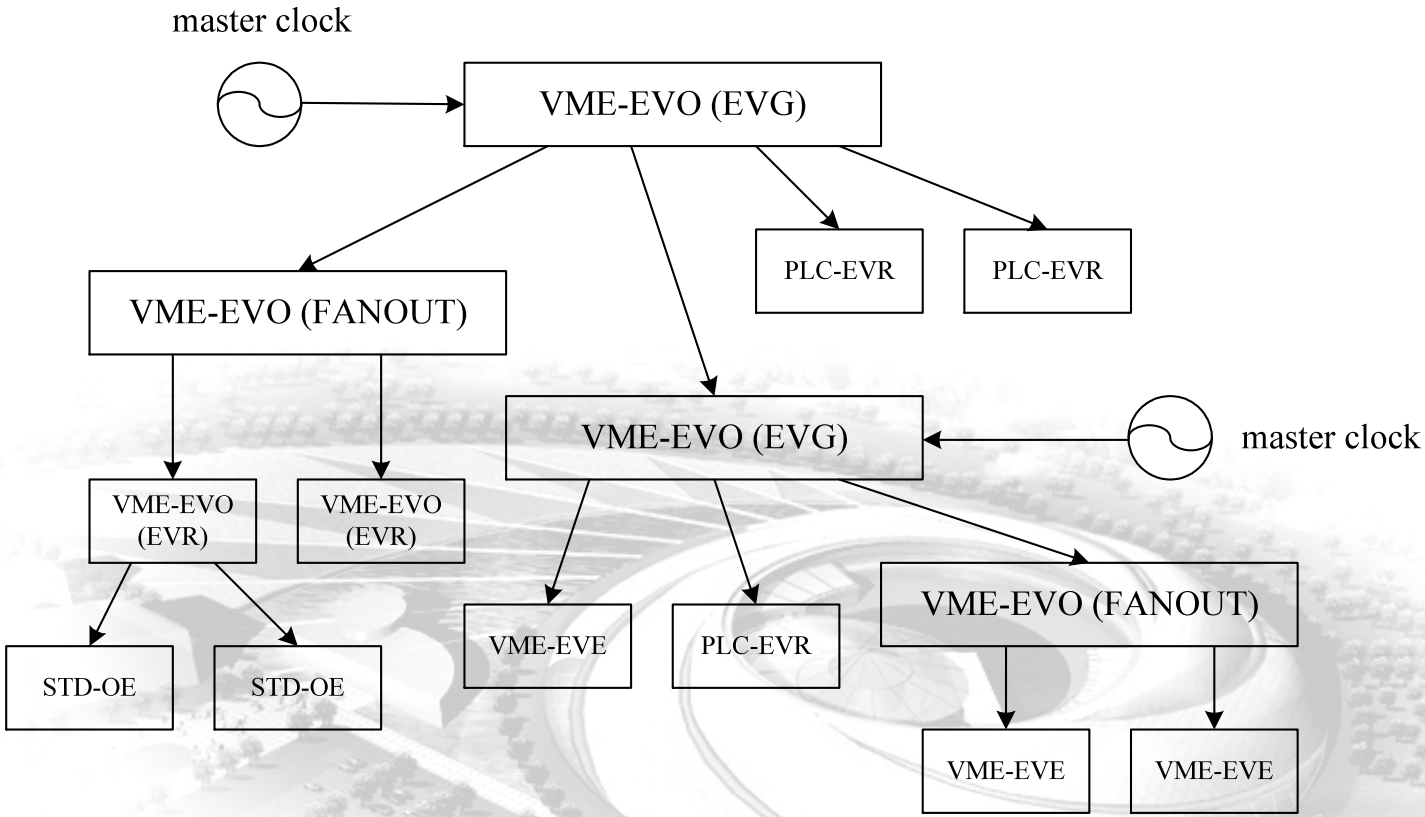
in Storage Ring





in Kicker station

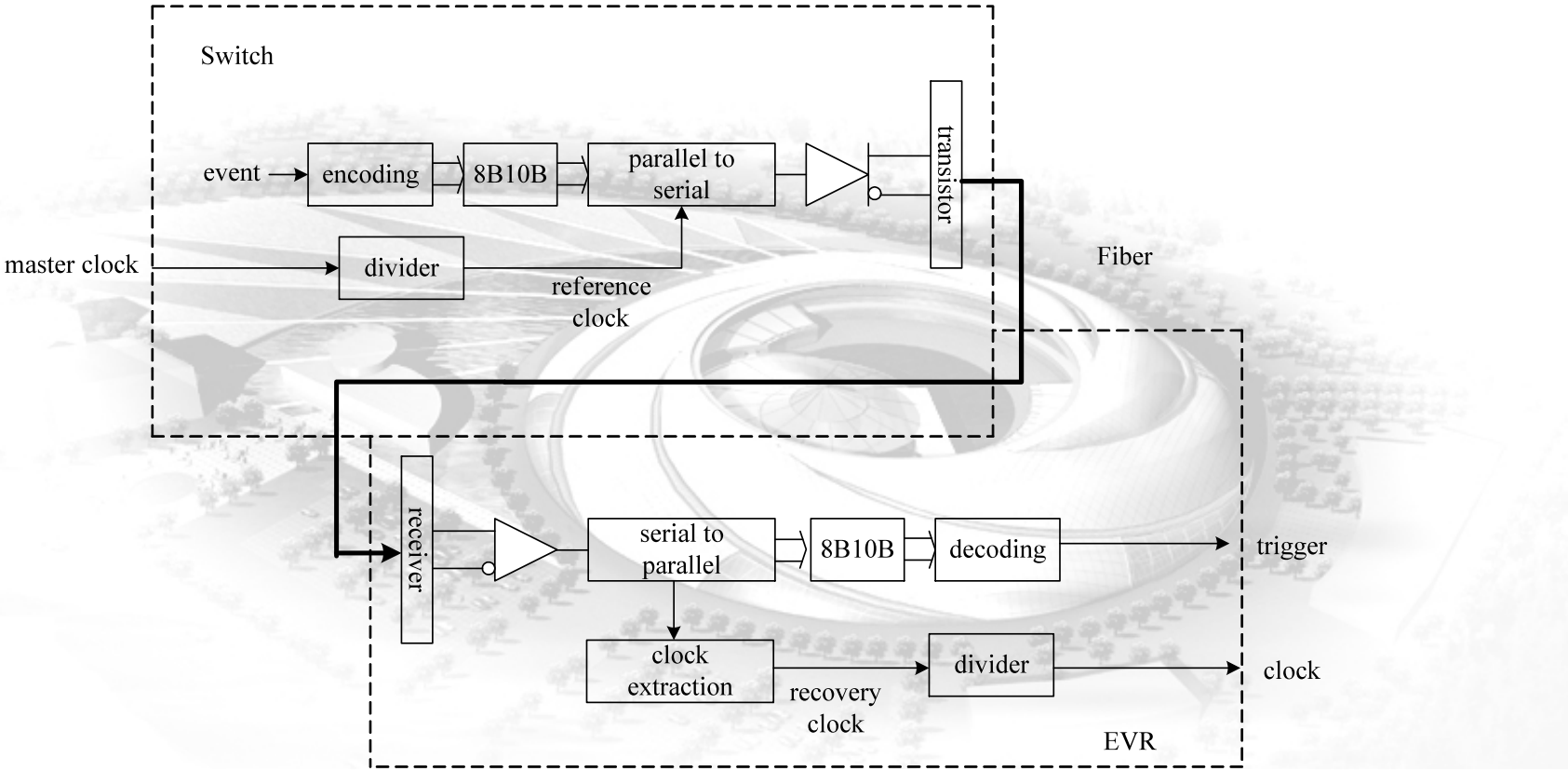
SINAP v2 timing system structure



System Design

- Synchronization

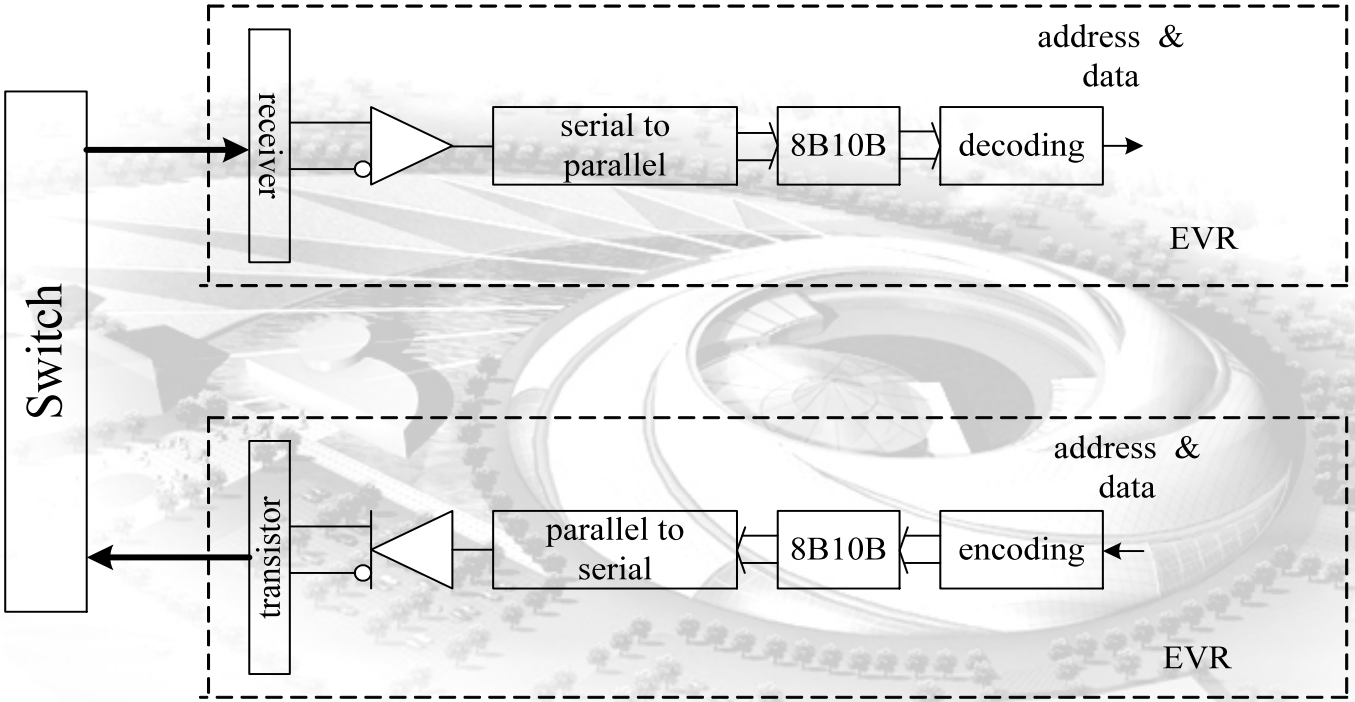
Broadcasting mode



System Design

- Deterministic Data Transfer

Switching mode



System Design

- Frame Format

1 byte for trigger code

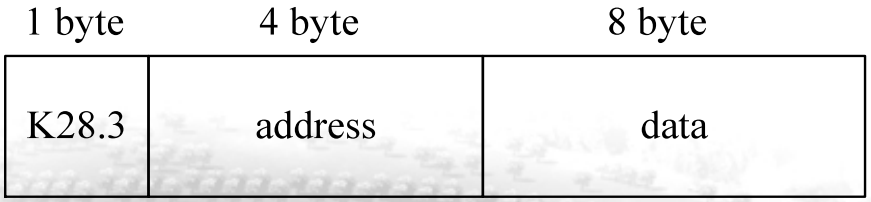
1 byte for data frame

1 byte	1 byte
trigger	data frame
K28.5	data frame
K28.5	data frame
K28.5	data frame
trigger	data frame
K28.5	data frame
⋮	⋮

The minimum interval of trigger is 8ns (2.5Gbps).

System Design

- Data Frame Format



4 bytes for address; 8 bytes for data; 1 byte for K28.3

The maximum data transfer rate is 76.9MB/s (2.5Gbps)

Hardware list

- SINAP v2 timing system:
  - VME-EVO
  - VME-EVE
  - PLC-EVR
  - STD-OE

VME-EVO

Configured to EVG, EVR and FANOUT by software

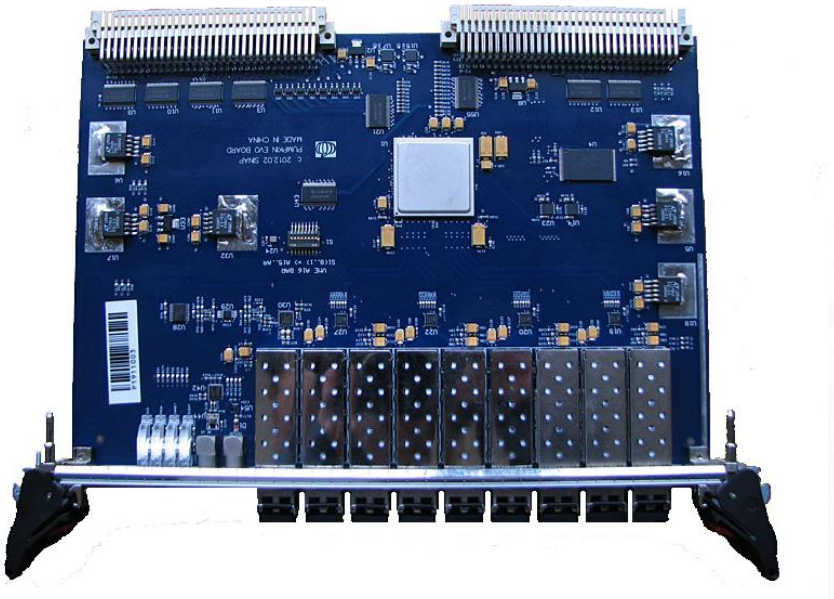
VME 6U module, A16D32 addressing

Input: 1 RF clock (0 – 10dBm)

1 interlock / AC-line (TTL)

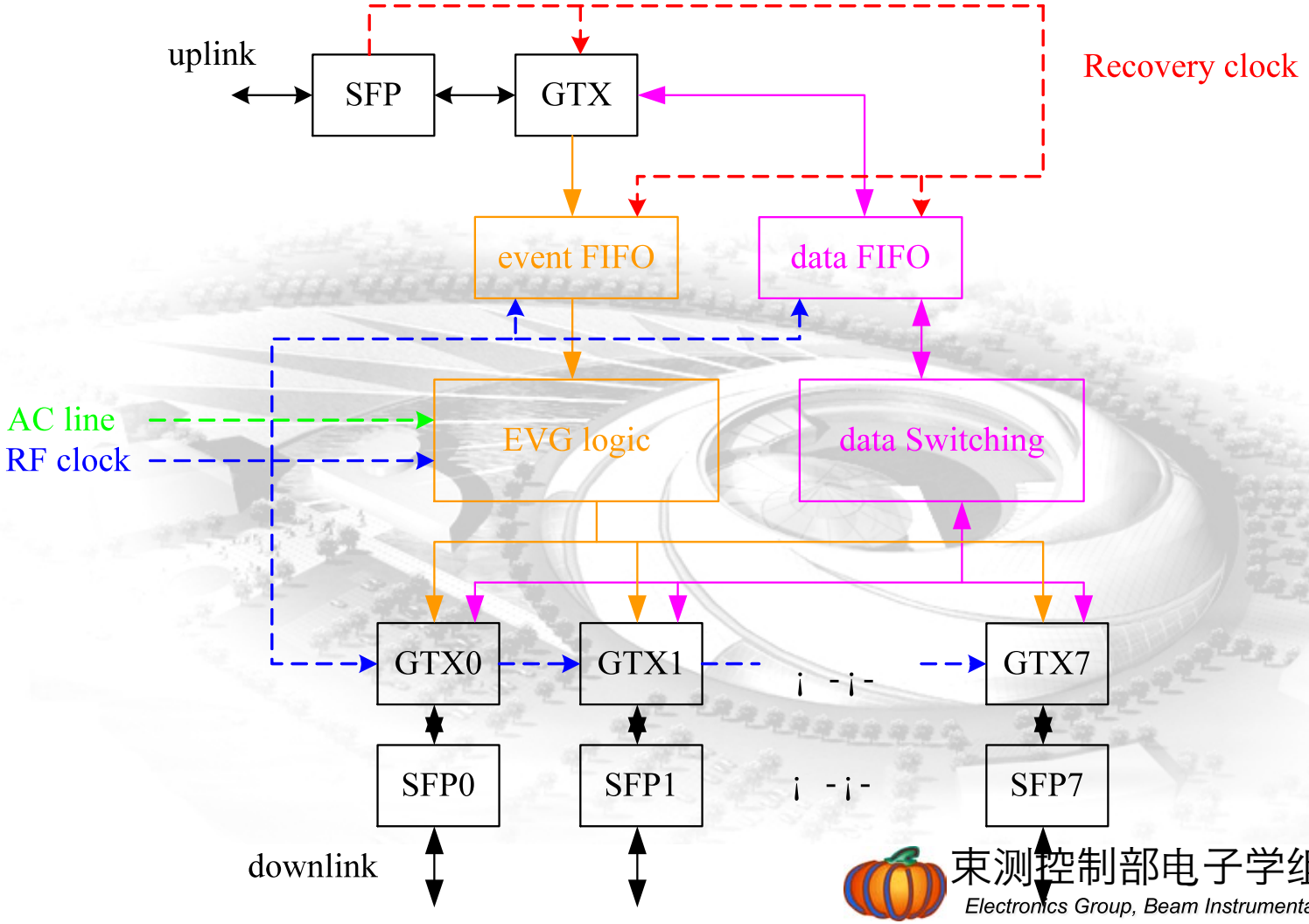
1 fiber (SFP module)

Output: 8 fiber (SFP module)



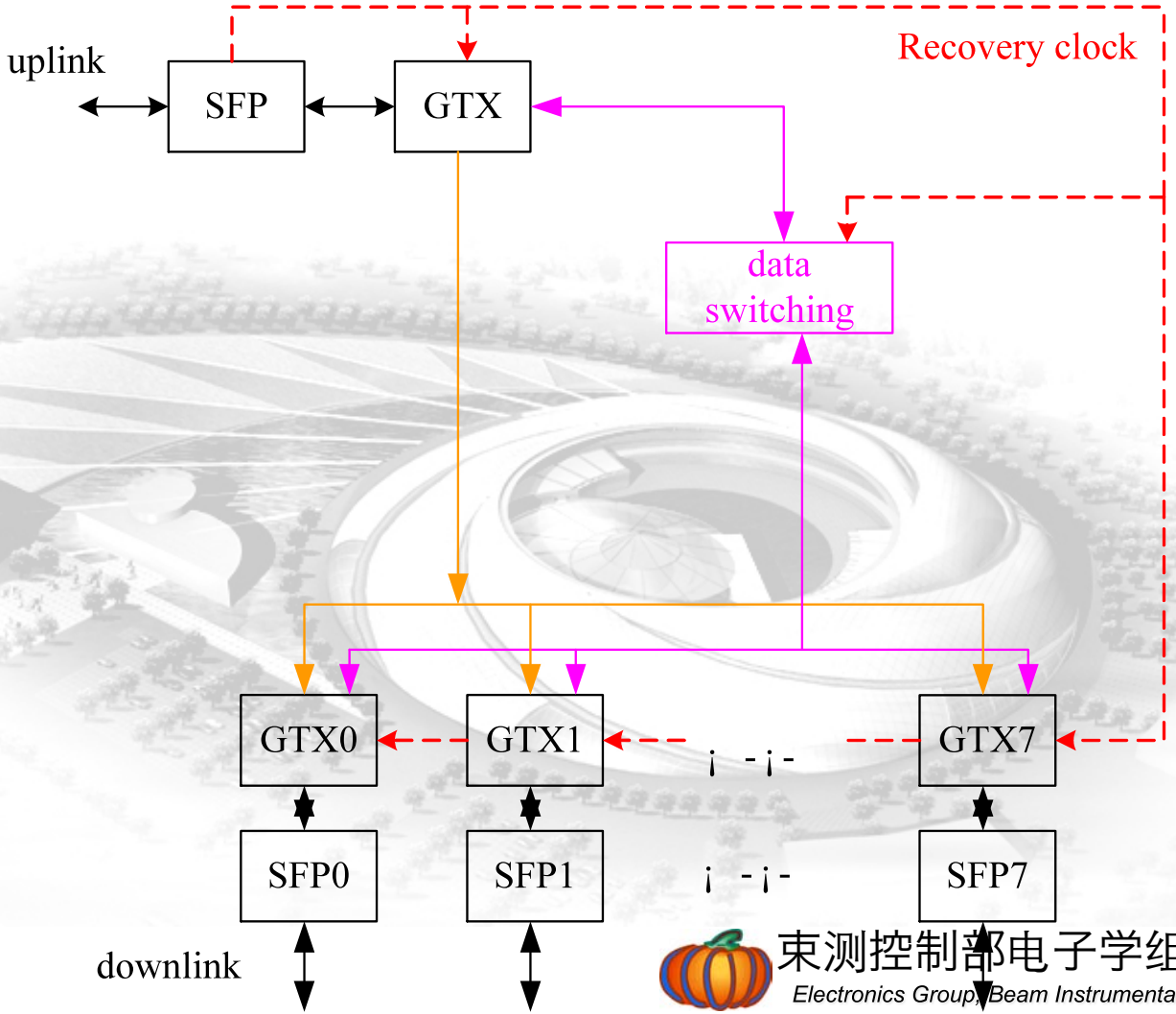
VME-EVO

- Configure to EVG



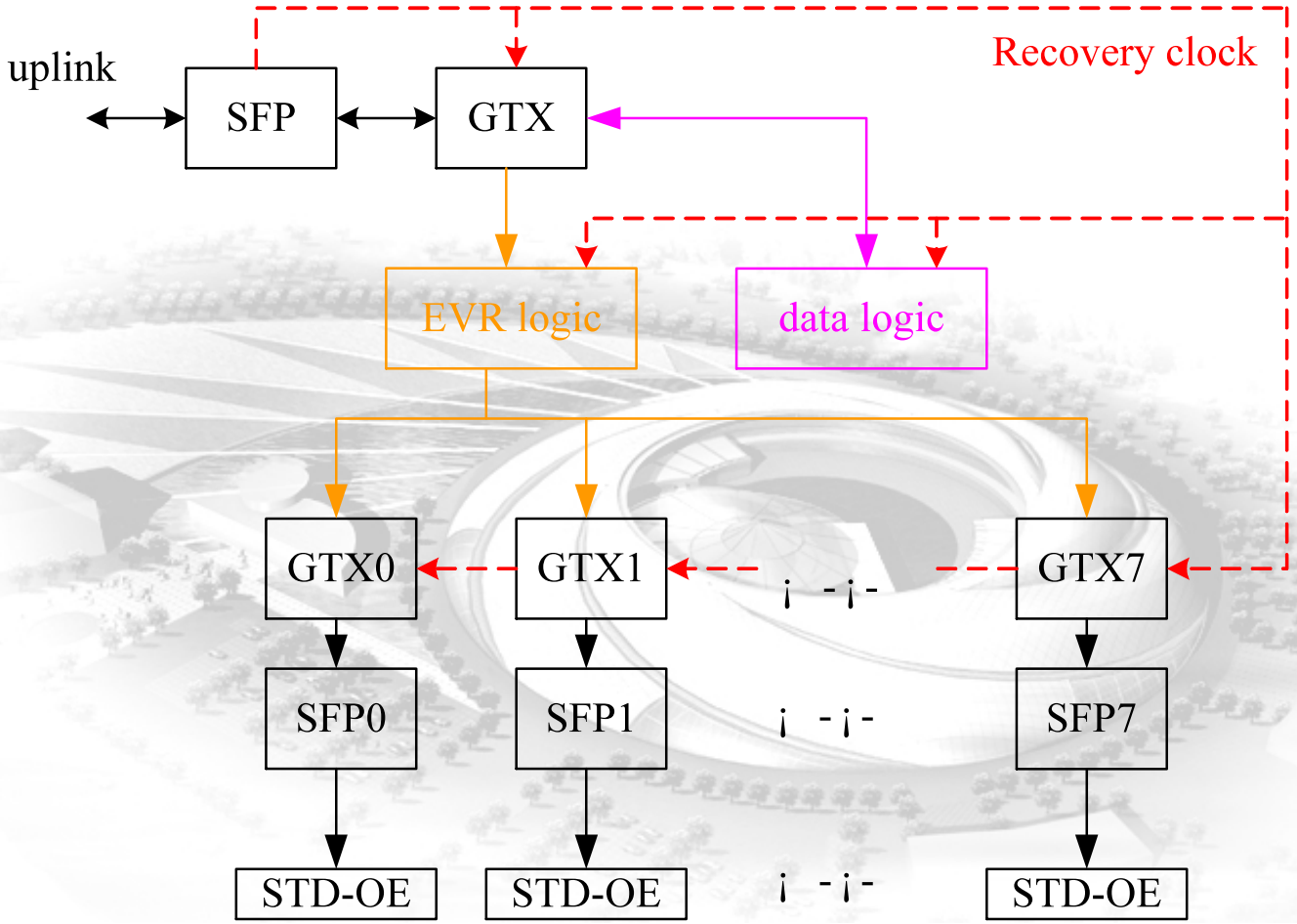
VME-EVO

- Configure to FANOUT



VME-EVO

- Configure to EVR



VME-EVE

Configured to EVR

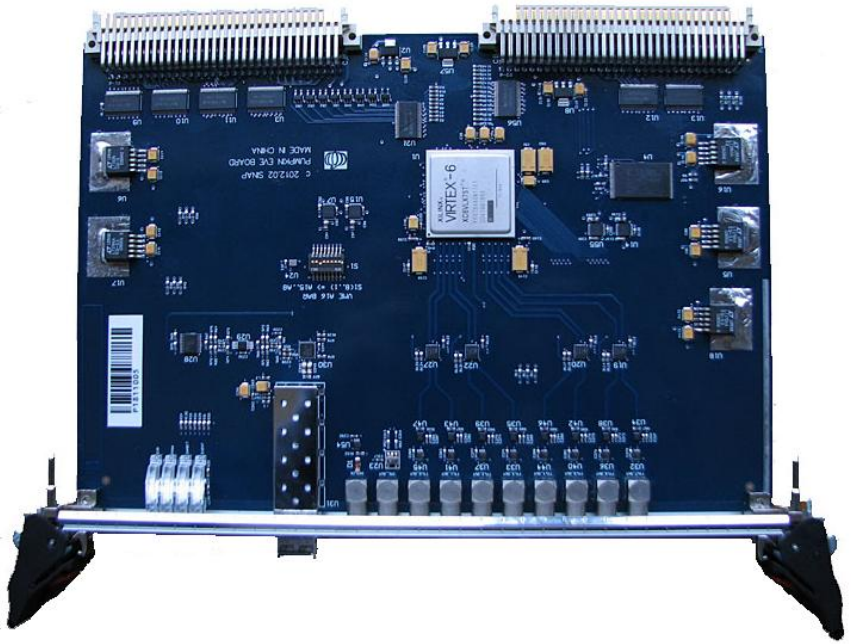
VME 6U module, A16D32 addressing

Input: 1 interlock (TTL)

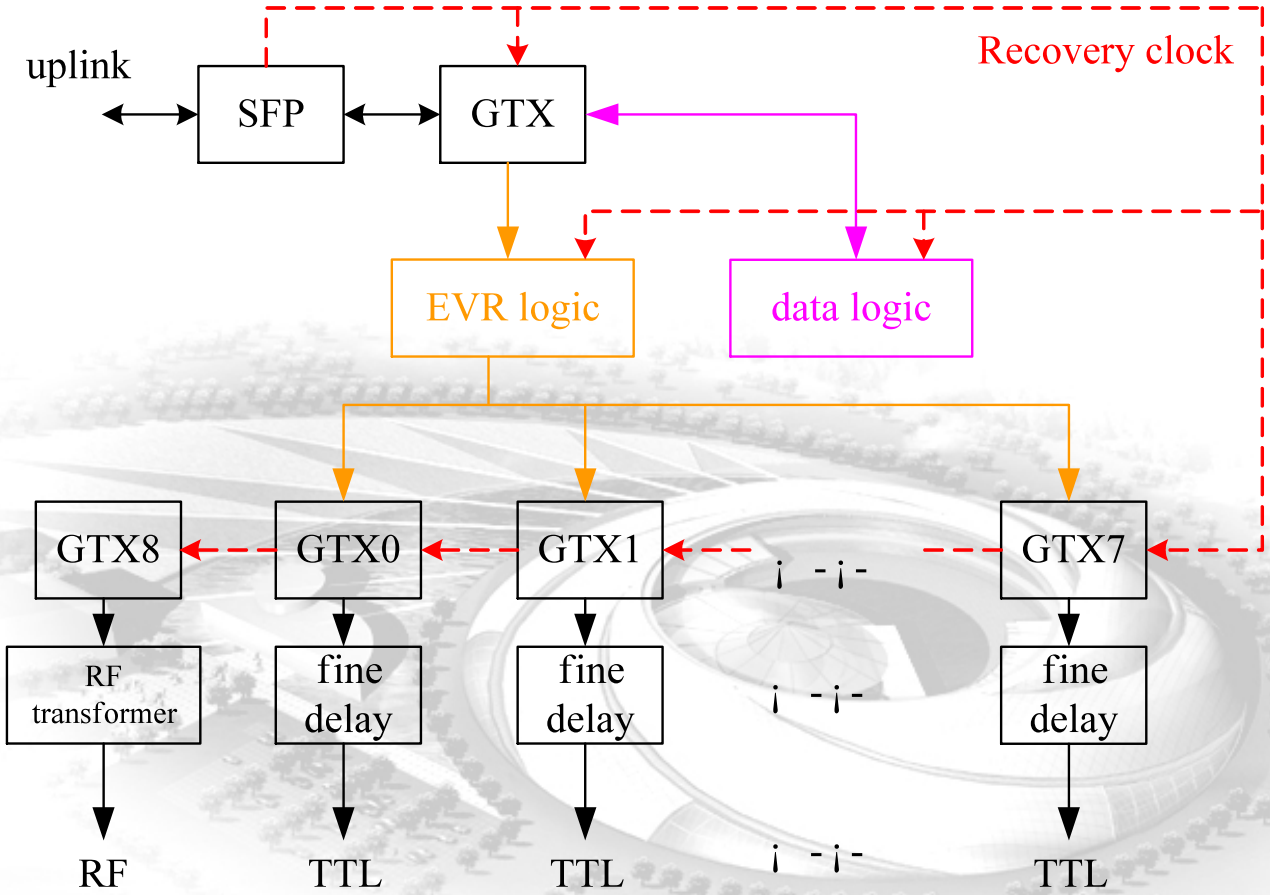
1 fiber (SFP module)

Output: 8 outputs (TTL)

1 RF recovery clock

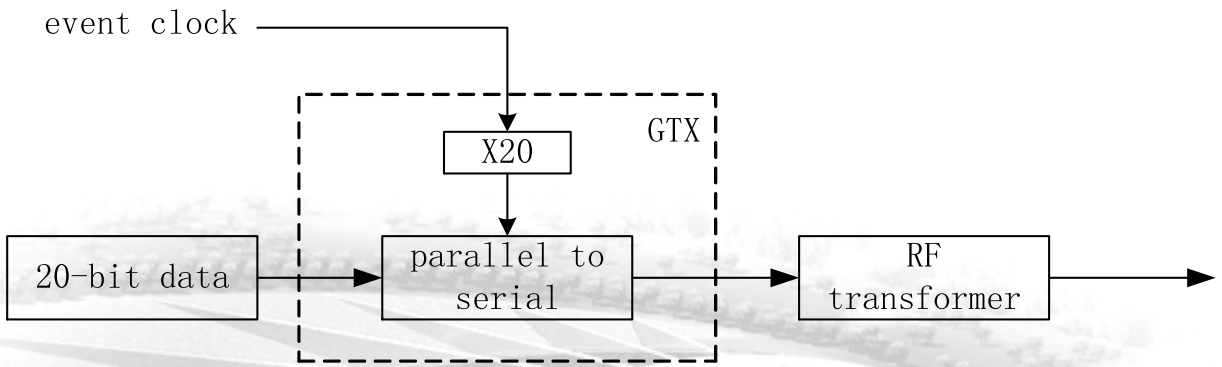


VME-EVE


uplink
SFP
GTX
Recovery clock
EVR logic
data logic
GTX8
GTX0
GTX1
GTX7
RF transformer
fine delay
fine delay
fine delay
RF
TTL
TTL
TTL

VME-EVE

- RF recovery clock



0x003ff -> event clock

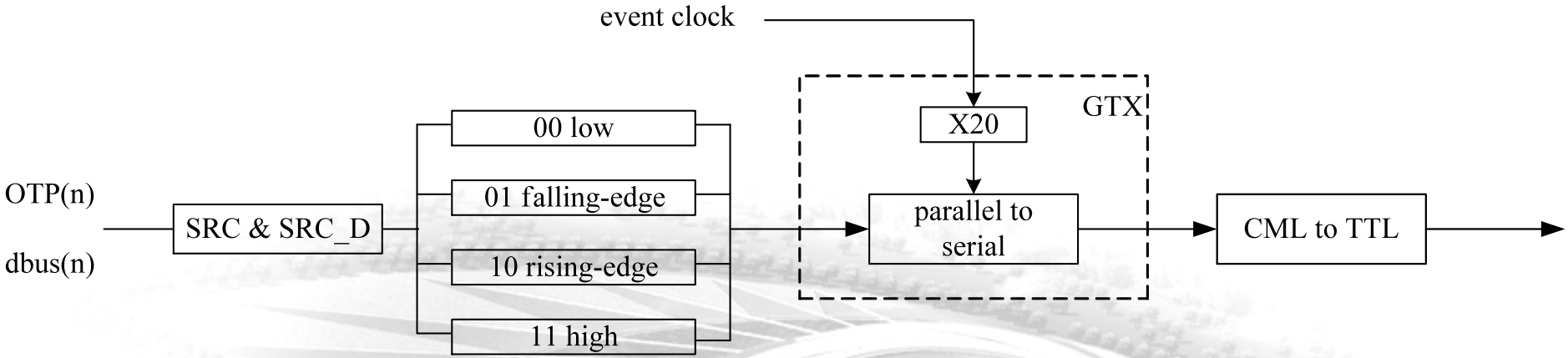
0x03c1f -> 2x event clock

0x18c63 -> 4x event clock

…

VME-EVE

- RF delay



(0,0,0xfffff,0xfffff) -> (0,0x1,0xffffe,0xfffff)

1/20 event clock delay

(Synchronized with RF clock)

PLC-EVR

Yokogawa FAM3 series, 1-slot module

Input/Output register mode

external 5V/3A DC power supply is required

Input: 1 fiber (SFP module)

Output: 4 outputs (TTL)

STD-OE

19 inches 1U standard chassis

110/220V 50-60Hz AC power supply

Input: 4 fiber (SFP module)

Output: 4 outputs (TTL)